EURASIP SEMINARS

"Hardware Design of DSP Systems"

Date: 8th February 2012

Venue: Escuela Ténica Superior. Universidad San Pablo CEU-Madrid

Organized by Gabriel Caffarena (Eurasip Local Liaison Officer, Associate Professor Universidad San Pablo CEU)

The seminar was oriented to both researchers from academia and hardware engineers from industry. The first talk was about low-power design techniques for FPGAs, by Eudardo Boemo from the Universidad Autonoma de Mardrid, where the state of the art was reviewed and 22 low-power “design tips” were recommended. A comparison of different techniques from academia and industry (Xilinx, Actel and Altera, etc.) were given. The talk focused on application-specific hardware architectures and also on processors. The second talk addressed the design challenges of 28-nm technology microchips, focusing on process variation, presenting hardware design techniques to account for performance variability. Run-time power consumption control for the next generation of microprocessors was explained. It was given by Ruzica Jectiv, from Berkeley Wireless Research Center/Universidad Politecnica de Madrid.

A total of 38 people attended: 11 researchers/professors, 10 hardware designers from industry and 17 undergraduate students. There were professors and Engineers from Universidad San Pablo CEU, Universidad Politécnica de Madrid, Universidad Autónoma de Madrid, the Spanish Aerospace Institute (INTA), the Spanish Center of Energy and Environment Research (CIEMAT), Madrid Deep Space Communications Complex-NASA and companies from the aerospace, electronics and telecommunications industries (INDRA, Thales-Alenia-Space, RBZ, NIT) . We can consider the seminar a total success.

The two lecturers with Gabriel Caffarena in the middle