Design Considerations of Ultra-Low-Voltage Self-Calibrated SAR ADC

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Abstract—**This paper discusses the design of 0.5V 12bit successive approximation register (SAR) analog-to-digital converter (ADC) with focus on the considerations of self calibration at low supply voltage. Relationships among noises of comparators and overall ADC performance are studied. Moreover, an ultra–low-leakage switch is demonstrated in a 0.13μm CMOS process and an improved process of measuring mismatch is proposed to alleviate the charge injection of sampling switch. Simulation shows the ADC achieves an ENOB of 11.4b and a SFDR of 90dB near Nyquist rate with capacitor mismatch up to 3%. At 12b 1MS/s, the ADC exhibits an FOM of 13.2fJ/step under 0.5V supply voltage.**

I. INTRODUCTION

ENERGY- constrained applications such as mobile devices, wearable medical equipments, wireless sensor networks, etc., require power-efficient analog-to-digital converters (ADC) for long life span. Meanwhile, low voltage ADC was demanded by the continuous down-scaling of digital supply voltage for SoC integration. In these applications, successive approximation register (SAR) ADC is normally a dominant architecture due to its low power and mostly-digital characteristics [1] [2].

The achievable resolution of SAR ADC at normal voltage is mainly limited by capacitor matching. Benefiting from the down-scaling of CMOS technology, however, SAR ADC can incorporate additional calibration logic naturally. Several calibration techniques have been reported [3]-[6], whereas there is few designs discussing the design considerations of high resolution sub-1V ADCs with the calibration. Improved results of the calibrations in [3], [4] and [5] were reported with supply voltages above 1V. The ADC in [6] works at 0.5V supply voltage with an ENOB around 10b after the calibration.

Ultra-low-supply voltage introduces some additional serious challenges to the self-calibrated SAR ADC. The noises of the comparators play more dominant roles in limiting the ADC's performance at low voltage compared with that at normal voltage. And the improved performance due to the calibration is also degenerated significantly as the measurement of capacitor's mismatch is vulnerable to the leakage and the charge injection of sampling switches and the offset of the comparator.
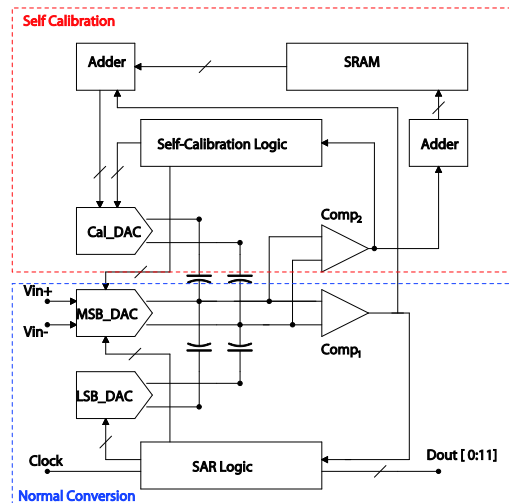
Fig. 1. The architecture of self-calibrated ADC.

This paper elaborates the design considerations of SAR ADC with self calibration at low voltage. Relationships among noises of comparators and overall ADC performance are studied. Meanwhile, we discuss challenges to circuit designs of ultra-low-voltage ADC with self calibration and present several solutions. Simulated in 0.13μm CMOS process, the implemented 0.5V ADC achieves 11.4b ENOB and 13.2fJ/step FOM with capacitors' mismatches up to 3%.

II. SELF CALIBRATION OF SAR ADC

Fig. 1 shows the block diagram of the self-calibrated SAR ADC. The ADC consists of two comparators, a main DAC (splitting to MSB DAC and LSB DAC), a calibration DAC, SAR logic, self-calibration logic, adders and SRAM. The modules in the bottom of Fig. 1 are responsible for normal SAR conversion while those in the top are in charge of the self calibration.

Once the ADC is powered on, the measurement of the mismatch is started under the control of self-calibration logic. The measurement begins from the MSB capacitor in the MSB DAC and ends at the LSB capacitor. To begin with, all capacitors except the capacitor ready for the measurement in the main DAC samples reference voltage V_{ref} and then redistribute the charge with the capacitor ready for the measurement, resulting in the residual voltage related to the mismatch [3]. Then the calibration DAC digitizes the residual voltage in a SAR conversion making use of the precise comparator $Comp_2$.
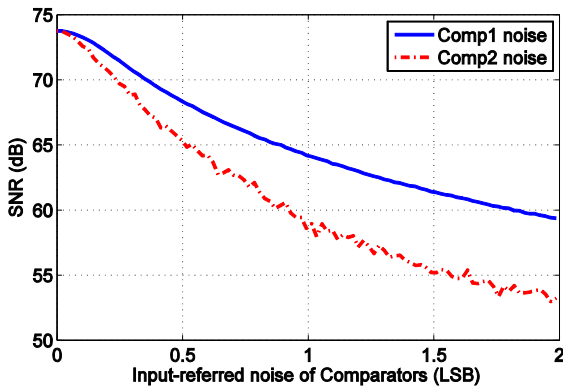
Fig. 2. SNR of 12bit self-calibrated ADC as functions of the comparators' noises.

The digital code of the residual voltage is processed by adders and stored in the on-chip SRAM, thus the measurement of one capacitor's mismatch is accomplished. This procedure repeats subsequently until the LSB capacitor in MSB DAC is completed.

After the measurement of the mismatch, the normal conversion begins and the mismatch-measurement block is powered off. During the normal conversion, the calibration DAC adjusts its connection according to the output of $Comp_1$ and the accumulation result of the data read from the SRAM. Effectively, the error voltage caused by capacitors' mismatches is compensated by the calibration DAC and the accurate successive approximation could be established.

III. NOISES CONSIDERATIONS

For 12bit SAR ADC at 0.5V voltage, the 1LSB voltage is very small (244uV) and the input-referred noises of $Comp_1$ and $Comp_2$ would degenerate the ADC's performance drastically. As a result, it is very necessary to analyze how the two noises deteriorate the ADC's performance.

Because the $Comp_1$ is connected to the output of DAC in the normal conversion, its noise could be seen as one part of the input signal. As for the noise of $Comp_2$, it introduces some errors to the measurement of the capacitor's mismatch, resulting in the incomplete compensation to the capacitor's mismatch in the normal conversion. Consequently, the noise of $Comp_2$ could be converted to the mismatch-induced error of the ADC by some ratio. Therefore, the relationship between the two noises and the ADC's SNR would be demonstrated as

$$SNR = 10 * \log(\frac{(\frac{2^N \Delta}{2\sqrt{2}})^2}{\frac{\Delta^2}{12} + V_{n,1}^2 + V_e^2})$$

$$= 10 * \log(\frac{(\frac{2^N \Delta}{2\sqrt{2}})^2}{\frac{\Delta^2}{12} + V_{n,1}^2 + k^2 V_{n,1}^2}). \quad (1)$$
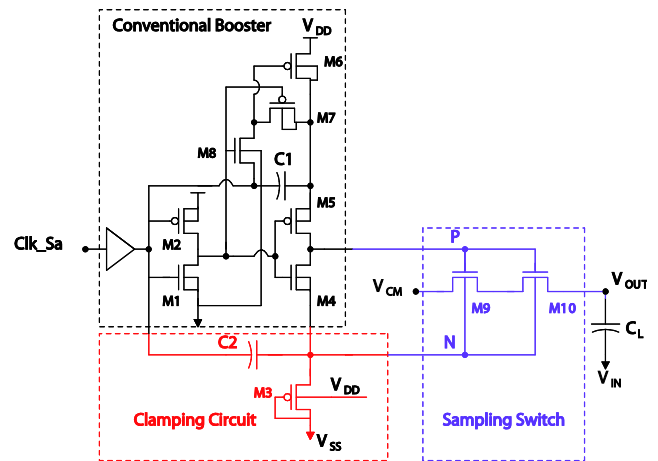

Fig. 3. Schematic of the sampling switch in SAR ADC.

Where $V_{n,1}$ and $V_{n,2}$ are the input-referred noises of $Comp_1$ and $Comp_2$, respectively. Δ is the value of 1LSB voltage and k is the conversion factor from $V_{n,2}$ to V_e (the mismatch-induced error).

In order to verify the analysis, a behavioral simulation of SAR ADC based on self calibration was performed. In the simulation, the values of unit capacitors in MSB DAC were taken to be Gaussian random variables with standard deviation of 3%.

Fig. 2 shows SNR of the ADC as functions of two comparators' noises. As expected, the noises of $Comp_1$ and $Comp_2$ both degrade the SNR nearly exponentially and the relation between noises and SNR approaches the relationship displayed by equation (1). Besides, the noise of $Comp_2$ deteriorates the SNR more drastically than that of $Comp_1$, which is due to the fact that the digital codes of mismatches including noises are add to compensate the error voltage in the normal conversion. However, $Comp_2$'s noise could be averaged out by multiple measurements of the same mismatch. In this design, we set the noise parameters of 60μV for $Comp_1$ and 40μV for $Comp_2$ to ensure more than 11bit ENOB.

IV. CIRCUIT CONSIDERATIONS AND DESIGNS

At the circuit level, the challenges for the self-calibrated ADC under ultra low voltage lie in the leakage and the charge injection caused by the sampling switch and the input-referred offset of $Comp_2$. As a result, some techniques are presented to mitigate these interferences.

A. Ultra-low-leakage switch

For a SAR ADC operating at low voltage, the *on* resistance of sampling switch determines the bandwidth of SAR ADC while the leakage affects its linearity significantly. For self-calibrated SAR ADC, the *off* leakage would also distort the residual voltages in the measurements of mismatches and deteriorate the improved performance directly.

A ultra-low-leakage switch shown in Fig. 3 is proposed to mitigate the problem. The proposed switch is consisted of three parts, a conventional voltage booster, a voltage clamping circuit and a sampling switch. By producing a boosted voltage
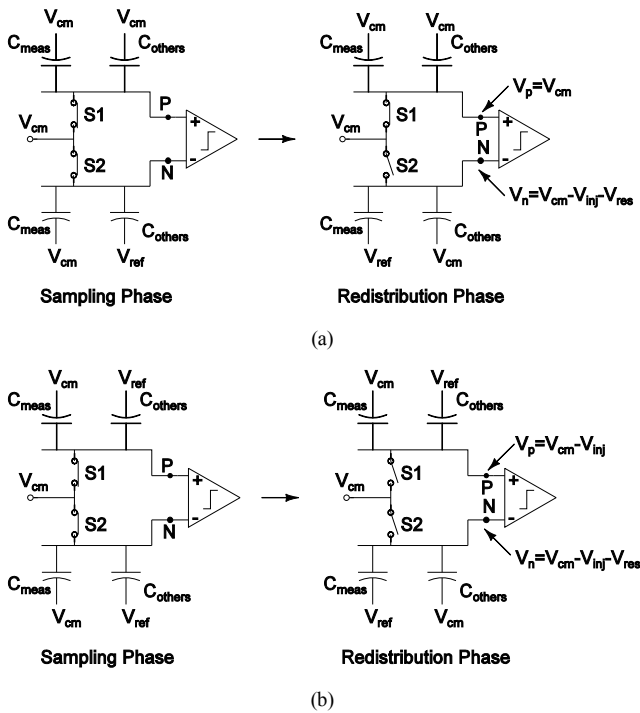
(a)

(b)

Fig. 4. The processes of digitizing the residual voltage: (a) the conventional and (b) the proposed. In the figure, V_{inj} is the voltage caused by charge injection and V_{res} is the residual voltage due to the mismatch between C_{meas} and C_{others}.

Fig. 5. The waveforms of V_p and V_n in Fig. 4 (b).

Fig. 6. Layout of the ADC.

at the *on* phase and a negative voltage at the *off* phase, it can decrease the *off* leakage and increase the *on* conductance simultaneously. When the sampling clock Clk_Sa is "1", the voltage at node N is a small positive value and the voltage at node P is approximately $2V_{dd}$, which improves the *on* conductance. If Clk_Sa turns from "1" to "0", the voltages at nodes N and P turn to a same negative level. This would result in a negative *off* voltage at the gate and increase threshold voltage due to the negative voltage at the bulk, reducing more *off* current than conventional voltage boosting [7].

B. The charge injection of sampling switch

Fig. 4 (a) shows the conventional process of measuring the residual voltage on the bottom array. During the process, S2 is turned off after V_{ref} is sampled by C_{others} in the bottom array while S1 is turned on all the time. Therefore, charge injections caused by the switch S2 would introduce an offset to the measurement of the residual voltage.

At low supply voltage (0.5V), the amplitude of the residual voltage due to the mismatch is very small. For example, if the MSB capacitor includes 3% mismatch, the residual voltage will have the largest value of 3.75mV [3]. Because the residual voltage combined with the offset voltage is digitized by calibration DAC, the large offset voltage compared with the residual voltage would saturate measurement results and thus bring about the failed self calibration.

To mitigate this interference, we optimize the process of digitizing the residual voltage as shown in Fig. 4 (b). Take the measurement of residual voltage on the bottom array for example. In the sampling phase, S1 and S2 in Fig. 4 (b) turn on
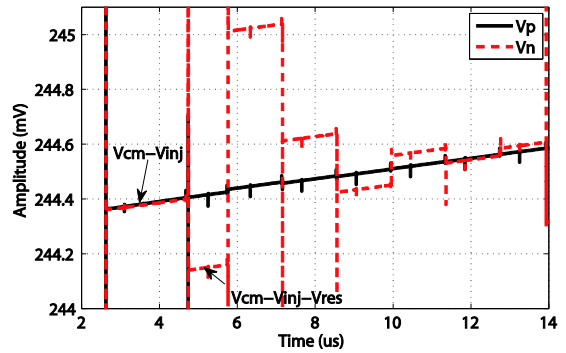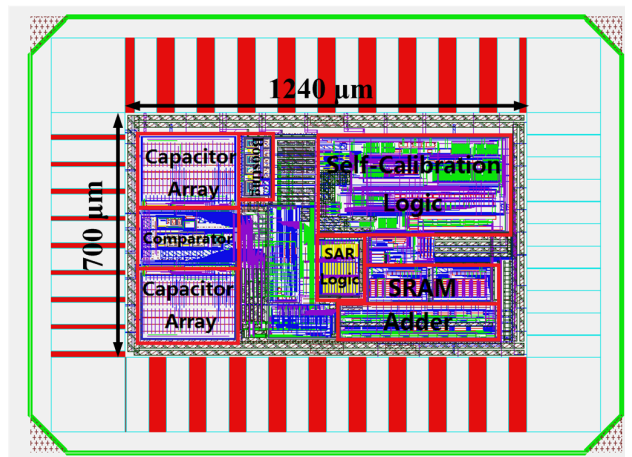
at the same time and both the top and bottom array samples V_{ref}. When it comes to the redistribution phase, S1 and S2 turn off simultaneously. Since S1 and S2 have the same dimensions and circuit connections of the top and the bottom arrays are the same, the charge injections caused by S1 and S2 are nearly equal. Subsequently, only the bottom array are reversed between V_{cm} and V_{ref} and generates the residual voltage whereas connections of the top array remain unchanged. Finally, the residual voltage is digitized in a SAR conversion with the help of calibration DAC.

In the proposed process, the residual voltage is digitized through successive comparison with V_{cm}-V_{inj} instead of V_{cm}, so the offset caused by charge injection would be compensated effectively and the impact of the charge injection is alleviated.

Moreover, the improved process could alleviate the impact of the sampling switch's leakage. Fig. 5 shows the simulated transient voltage waveforms at nodes N and P in the measurement. Because S1 and S2 are both turned off and V_p is close to V_n, the error voltage due to S1's leakage approaches that of S2, as shown in Fig. 5. Consequently, the leakage induced error voltage of S2 could be compensated by that of S1 effectively.

C. Comparator with offset cancellation

To digitize the small residual voltage with enough accuracy, $Comp_2$'s resolution should be very high. In this work, $Comp_2$ was implemented by two pre-amplifiers and a latch to ensure enough gain. Meanwhile, the output offset cancelation was exploited in $Comp_2$ to diminish the offset voltage and avoid the saturation of measurement results.

V. SIMULATED RESULTS AND DISCUSSIONS

A 12b 1MS/s SAR ADC at 0.5V has been implemented in a 0.13μm CMOS technology, occupying 1.2mm × 0.7mm active area. Fig. 6 shows the layout of the ADC. In the simulation at the circuit level, random capacitor mismatch up to 3% was adopted, which covers 99.7% of actual mismatch distribution with 1% of σ. And parasitic capacitors with the values of 3% are contained in the simulation.

A. Dynamic Performance

The dynamic performance of the ADC without calibration and that with calibration is shown in Fig. 7. The ENOB is improved from 9bit to 11.4bit by self calibration. What's more, SFDR of 90dB is achieved compared with 64.3dB before calibration. It could be clearly shown that the noises and circuit considerations in the preceding sections ensure the performance of self-calibrated ADC at low voltage.

B. Power Consumption and FOM

At sampling rate of 1MS/s, the ADC draws 35.7μW from a 0.5V supply voltage. The percentage of power consumption for digital logic, comparators and capacitor array are 37.2%, 56% and 6.7%, respectively. The less power consumption of capacitor array results from the small unit capacitance. In this design, more than half of the power is allocated to comparators due to the noise requirements.

The figure of merit (FOM) for Nyquist converters refers to the energy required to accomplish an effective conversion step. The FOM is defined as

$$FOM = \frac{Power}{2^{ENOB} \cdot f_s}. \qquad (2)$$

The FOM of the proposed ADC is 13.2fJ/conversion-step at 12b 1MS/s, which is a competitive value. The high power efficiency is partially a result of the low supply voltage that decreases the power of digital circuits quadratically. Meanwhile, due to the self calibration, the unit capacitance is able to be very small, decreasing the power of DAC significantly.

VI. CONCLUSIONS

This paper elaborates the analysis and design of a 12bit 1MS/s SAR ADC at 0.5V with self calibration. The effects of noises on the performance of self-calibrated ADC are demonstrated. Circuit considerations and designs on ultra-low voltage self-calibrated SAR ADC are also described. Simulated in a 0.13μm CMOS, the proposed ADC exhibits 11.4bit ENOB and 90dB SFDR with capacitor mismatch up to 3%. A re-
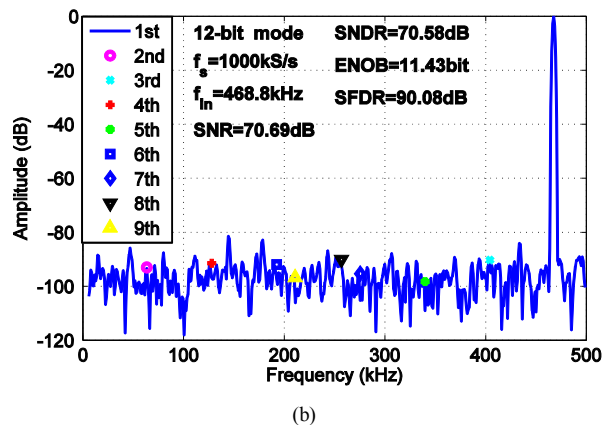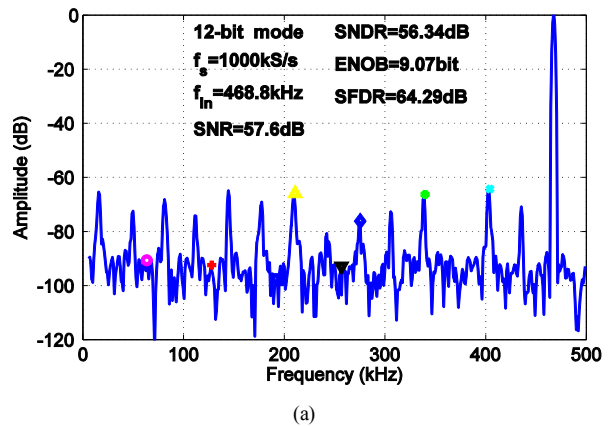

(a)

(b)

Fig. 7. Dynamic performance with a 468.8kHz input at 1MS/s sampling rate: (a) before calibration (b) after calibration.

markable power efficiency of 13.2fJ/step FOM has also been achieved.

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