Multi-Step Switching Methods for SAR ADCs

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***Abstract* - This paper presents multi-step capacitor switching methods for SAR ADCs based on precharge with floating capacitors and charge sharing. The proposed switching methods further reduce the transient power of the split monotonic switching method (an improved version of the monotonic switching method). Compared to the split monotonic switching, adding charge sharing achieves around 50% reduction in switching power. Using precharge with floating capacitors and charge sharing simultaneously, the switching power reduces around 75%. The proposed switching methods do not require additional intermediate reference voltages.**

I. Introduction

Deeply scaled CMOS technologies give analog-to-digital converter (ADC) designers low supply voltage and insufficient intrinsic gain. Among all kinds of ADCs, the successive-approximation-register (SAR) ADC seems to gain the most advantages in CMOS downscaling. A SAR ADC usually consists of sampling switches, a comparator, capacitor arrays and SAR logic. The SAR ADCs obtain digital representation of input signal by switching instead of amplifying in amplifier-based ADCs like the pipelined ADC. Improved metal implementation enhances metal-oxide-metal (MOM) capacitor matching. Digital SAR logic reaches higher speed and energy efficiency as CMOS technology continues to scale down. Recent publications show SAR ADCs achieve excellent power efficiency [1][2][3].

The accuracy of the SAR ADC mainly relies on capacitive digital-to-analog converter (DAC) design. In SAR ADCs, the binary-weighted DAC capture input signal on one side of capacitor arrays while C-2C and split DACs use both sides to process input signal. Thus, a binary-weighted DAC has better intrinsic linearity than the other two due to its better immunity against parasitic effects. Nonetheless, a SAR ADC using a binary-weighted DAC suffers from large input capacitance, resulting in large capacitor switching power which grows exponentially with ADC resolution.

This switching power of the DAC in SAR ADCs has been well analyzed in [4][5]. This paper proposes switching methods based on the split monotonic switching method [6]. The proposed methods further reduce the switching power. Section II introduces the monotonic switching method and its variant. Section III describes the switching techniques and the proposed methods. Section IV shows the analysis and behavioral simulation result. Section VI draws the conclusion.

II. The Monotonic Switching Method and Its Variant

Conventional SAR ADCs samples input signals onto bottom plates of the capacitor arrays. The switching power of capacitor arrays with bottom-plate signal sampling has been well analyzed in [4]. A SAR ADC using the monotonic switching method makes the top plates of the DACs connected to the comparator input and bottom plates to reference voltages [7]. The monotonic switching method samples input signals onto top plates of the capacitor arrays, as shown in Fig. 1. The advantages of this switching method include half unit capacitor count and one less switching compared to the conventional case. The main disadvantage of this method is the changing input common-mode voltage during bit cycling which affects the accuracy of the comparator. Thus, a variant of the monotonic switching method referred to as split monotonic switching method is invented [6]. Fig. 2 shows one of the capacitor arrays of the split monotonic switching method. A capacitor is split into two parts. For example, C_{1px} and C_{1py} in Fig. 2 are split by C_{1p} in Fig. 1. In the reset state, one is switched to the positive reference voltage V_{refp} and the other to the negative one V_{refn}. Once a compotator decision has made, the monotonic switching method only switches one capacitor in a capacitor array and the other capacitor array remains unchanged. For the split monotonic switching method, a capacitor array switches a sub-capacitor and the other array switches another sub-capacitor. Fig. 3 shows the waveforms at the top plates of the monotonic and split monotonic switching methods. The figure shows the split monotonic switching

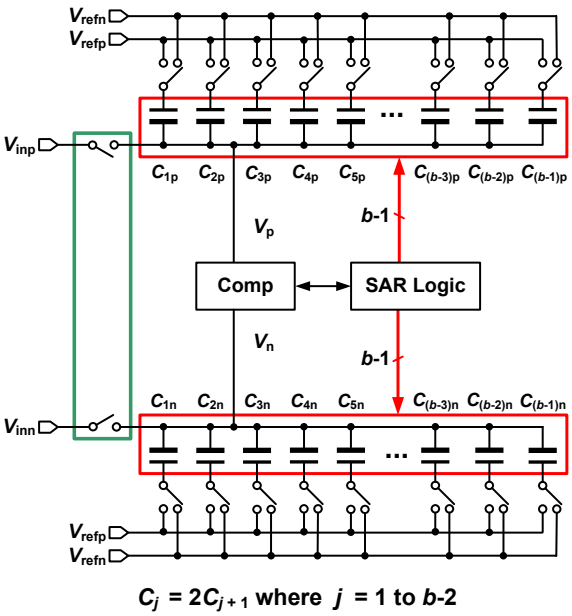

Fig. 1. A SAR ADC using the monotonic switching method.

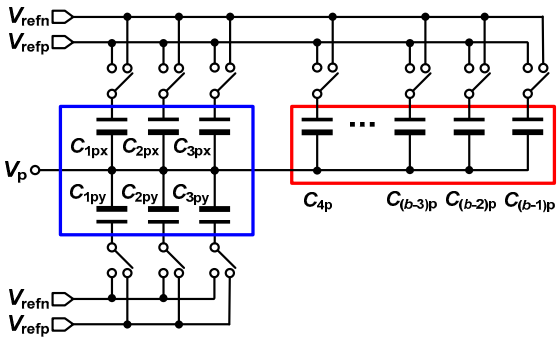

Fig. 2. The capacitor array of the split monotonic switching method.

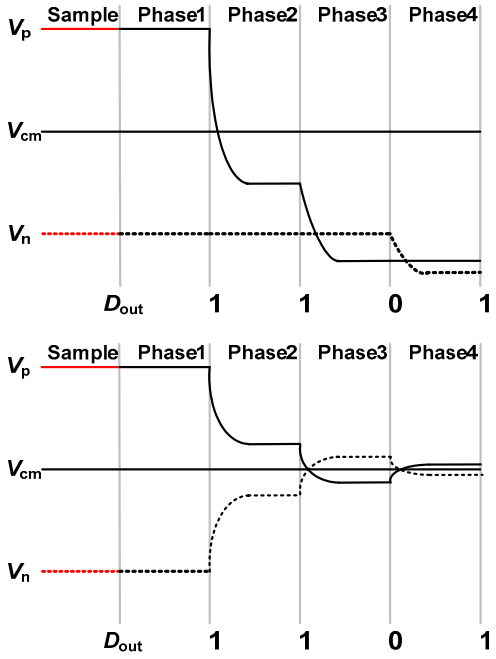

Fig. 3. The waveforms at top plates of the monotonic switching method (top) and the split monotonic switching method (bottom).

method has a constant common-mode voltage. Although doubled switches are required, the split monotonic method improves the accuracy of the SAR ADC. Generally, the split monotonic switching method only applies to the first several bits of a SAR ADC, and the rest bits perform monotonic switching. The compromised arrangement save hardware and enhance accuracy simultaneously.

The switching power of the capacitor array is proportional to the unit capacitance and the number of unit capacitors connected to the reference voltage. Intuitively, a high resolution capacitor array consumes more switching power than a lower one. For SAR ADCs with 10-bit or larger capacitor array, further switching power reduction is necessary to enhance power efficiency.

III. Proposed Multi-Step Switching Methods

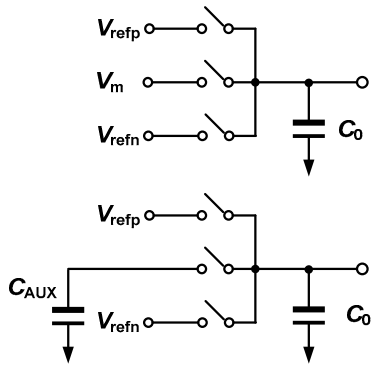

Fig. 4. Multi-step charging w/ external voltage (top) and that w/ a floating capacitor (bottom).

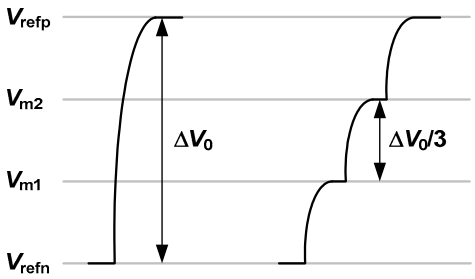

Fig. 5. Waveform of the one-step charging (left) and waveform of the multi-step charging (right).

This section shows two techniques reducing the energy consumed during capacitor transient activities. They are precharge with floating capacitors and charge sharing.

A. *Precharging with Floating Capacitors*

The power dissipation of a reference source arises from the charges to make a capacitor reaching the desired voltage level. In the split monotonic switching method, for each bit, a sub-capacitor is switched from V_{refp} to V_{refn}, and the other sub-capacitor is switched in the reversed direction. Charges from high voltage potential directly flowing to a lower voltage potential is energy inefficient. If the charges at the higher voltage potential help the charging of the capacitor at the lower potential, the charge recycling reduces the energy dissipation of the reference source. Generally, the charging of a capacitor is 'one-step.' However, a 'multi-step' charging is much more energy efficient. The multi-step charging idea is firstly mentioned in [8], and then applied to the drivers for LCD panels [9]. A SAR ADC employs this technique achieving excellent power efficiency [10]. This technique separates a 'one-step' charging into multi steps and multi phases, as shown in Fig. 5. If the voltage difference before and after charging is V_0 and the capacitance is C_0, the total energy consumed is $C_0V_0^2$ [4]. If the voltage difference is equally separated into n parts, the total energy is reduced to $C_0V_0^2/n$ where n is a natural number [8]. If the intermediate voltages are applied by power ICs, the efficiency loss during power conversion reduces the effectiveness of multi-step charging.

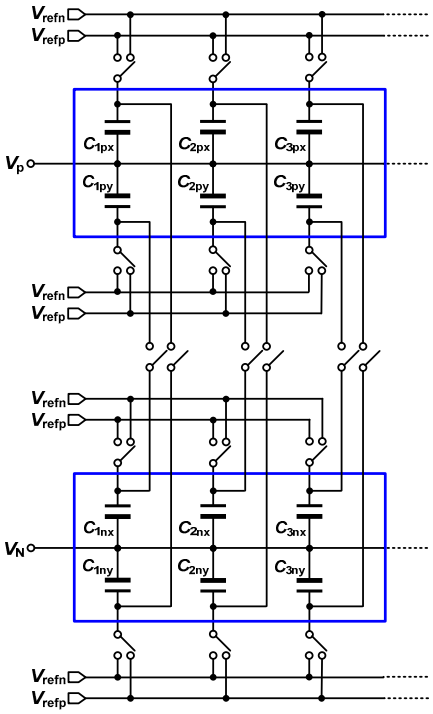

Fig. 6. The capacitor arrays of the split monotonic switching method combining charge sharing method.

Another approach is to use auxiliary capacitors to replace intermediate voltage sources. Fig. 4 depicts the cases using an external voltage (top) and a floating capacitor (bottom). In the bottom case, before switching to the highest voltage, the capacitor switches to the top plate of the floating capacitor. By repeating charging and discharging, the top plate of the auxiliary capacitor forms a stable intermediate voltage [9]. The auxiliary capacitor should be larger than the loading capacitor. A large ratio keeps the intermediate voltage stable.

In the multi-step charging procedures, the charges of intermediate steps are provided by the floating capacitors. Thus, the reference voltage only deals with the last charging. The more charging stages result in better energy efficiency. However, too many charging/discharging phases slow down the operation speed. Additional logic and driving circuits are also necessary to perform the multi-step charging/discharging.

B. *Charge Sharing*

Charge sharing is relatively intuitive. For example, a capacitor will discharge to the low voltage potential and the other identical capacitor will charge to the high potential. If we connect the top plates of the two capacitors together, the top plates will reach a middle voltage potential. Without dissipating charges from the reference voltage, the DAC array obtains free charges. Charge sharing needs less hardware than the precharge with floating capacitors. In split monotonic method, when a sub-capacitor switches upward, a sub-capacitor in the other array switches downward. The condition is perfectly suitable for charge sharing.

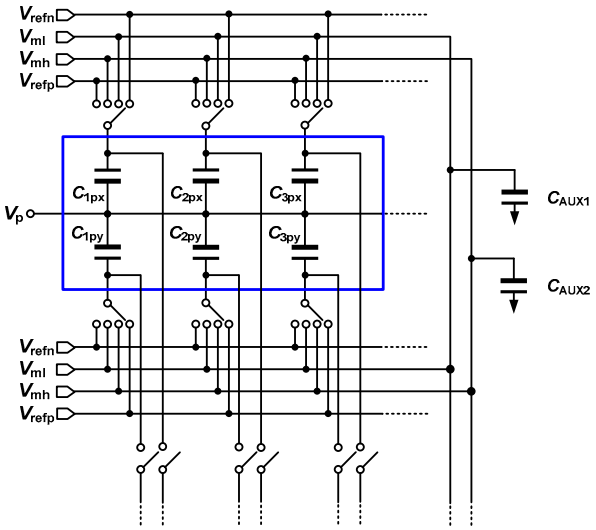

Fig. 7. The capacitor arrays of the split monotonic switching method combining charge sharing and precharge methods.

C. *Proposed Switching Methods*

Fig. 6 depicts the capacitor arrays of the split monotonic switching method combining the charge sharing technique. Note there is a switch placed between two sub-capacitors of the two arrays. The switches are used to perform charge sharing of two sub-capacitors. Fig. 7 shows the capacitor arrays of the split monotonic switching method combining charge sharing plus precharge with floating capacitors. Fig. 7 has three inter-stages. Floating capacitor performs the first and third charging and discharging; the charge sharing deals with the second one. Fig. 8 shows the waveforms of the bottom plates of the capacitor array using one charge sharing (left) and the waveforms using one charge sharing and two precharge (right). Note the inter-stage charging and discharging do not affect the final values.

Since the charge sharing and precharge with floating capacitors complicate logic design, the two techniques do not have to apply to the whole array. For a binary DAC array, the first 2- to 4-bit switching using the two techniques will save most of the switching power. For small capacitors, the two techniques are inefficient. The combined method is more suitable for low-speed high-resolution SAR ADCs. The method in Fig. 6 (only one charge sharing) is suitable for high-speed SAR ADCs.

V. Analysis and Behavioral Modeling

This section analyzes the switching power of the aforementioned switching methods. The switching power for each code of the monotonic switching can be expressed as

$$E_{\text{mono}}(n) = V_{\text{ref}} \times \left(V_{\text{x1}}(n) - V_{\text{x2}}(n)\right) \times C_{\text{ref}}(n) \quad (1)$$

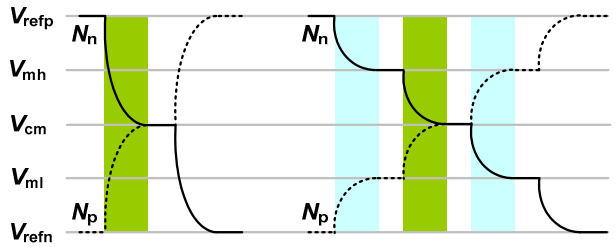

Fig. 8. The waveforms of the bottom plates of the capacitor array using one charge sharing (left) and the waveforms using one charge sharing and two precharge (right).

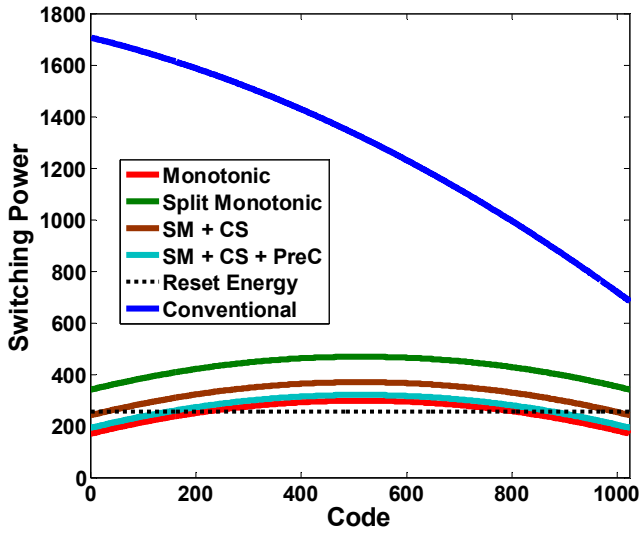

Fig. 9. Behavioral simulation result.

where $V_{x1}(n)$ and $V_{x2}(n)$ are the top-plate voltages before and after conversion for code n, respectively. C_{ref} is the total capacitance connected to V_{ref} after conversion. The switching power of the split monotonic switching can be expressed as

$$E_{mono\_split}(n) = V_{ref} \times \left(V_{x1}(n) - V_{x2}(n)\right) \times C_{ref}(n) + V_{ref}^2 \times C_{up}(n) \quad (2)$$

where C_{up} is the upward switching capacitance. The switching power of the split monotonic switching plus charge sharing and precharge with floating capacitors can be expressed as

$$E_{ms+cs+prec}(n) = V_{ref} \times \left(V_{x1}(n) - V_{x2}(n)\right) \times C_{ref}(n) + V_{ref} \times \left(V_{ref} - V_t \times \left[(C_{total} - C_{up}) / C_{total}\right]\right) \quad (3)$$

where $V_t = V_{ref}/2$ for charge sharing case and $V_t = 3V_{ref}/4$ for charge sharing plus precharge case. (1) – (3) only show the switching power during conversion. (2) and (3) must add energy consumption in sampling (reset) phase. The value is $V_{ref} \cdot C_{ref,smp}$ where $C_{ref,smp}$ means the total capacitance connected to V_{ref} during the sampling phase. Note the monotonic switching does not consume energy during reset.

We use behavioral modeling to demonstrate the switching power reduction of the proposed switching methods. Fig. 9 shows the behavioral simulation result of five cases: 1) conventional switching; 2) monotonic switching; 3) split monotonic switching; 4) split monotonic switching with charge sharing; and 5) split monotonic switching with charge sharing and precharge. During conversion, the split monotonic consumes less reference energy than the monotonic switching. However, the monotonic switching method is the smallest if the energy consumption during sampling (reset) phase is added. Note the proposed methods consumed the smallest energy from reference buffer during conversion. Thus the reference buffer design becomes easier. The charge sharing and charge sharing plus precharge help the split monotonic switching to achieve significant switching power reduction.

VI. Conclusion

This paper proposes multi-step charging and discharging methods for the SAR ADCs based on the split monotonic switching. Although the split monotonic consumes more total energy, it dissipates less energy during conversion. Shift the settling issue of the DAC from conversion to reset is beneficial for high-speed operation. The reset phase is generally much longer than a bit conversion phase. The proposed methods do not require additional voltages. For a 10-bit SAR ADC, the total capacitance using the split monotonic switching is smaller than 2.5pF. On-chip auxiliary capacitors (>25 pF) are possible. The multi-step switching method not only saves switching power but also hardware cost.

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