DIGITAL CALIBRATION OF SAR ADC

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ABSTRACT

Four techniques for digital background calibration of SAR ADC are presented and compared. Sub-binary redundancy is the key to the realization of these techniques. Some experimental and simulation results are covered to support the effectiveness of these techniques.

Keywords—SAR ADC, digital background calibration, DAC mismatch, bit weight, sub-binary redundancy

1. INTRODUCTION

The return of switched-capacitor successive-approximation-register (SAR) analog-to-digital converter (ADC) has revealed the potential of the SAR conversion architecture in scaled technology for low-power operation [1]-[6]. Without the need for precision amplification, the analog operation of a SAR ADC is mostly switching type, similar to digital logic circuits. In addition, the single zero-crossing comparator employed in the bit-decision cycles is largely immune to offset errors, further reducing the analog design effort. One important trend in recent SAR works is the proliferation of the so-called *sub-binary* SAR architecture, which has fueled a continuous improvement on the conversion speed as well as the robustness of SAR.

In scaled technology, the signal-to-noise ratio (SNR) and linearity performance of SAR ADC are largely limited by the decreasing supply voltage and the static component mismatch errors of the digital-to-analog converter (DAC) used to produce the successive decision thresholds during the bit cycles. Consequently, while many recent SAR works have reported outstanding power efficiency, few demonstrate >10 effective number of bits (ENOB) [1]-[6].

In this paper, a few digital background calibration techniques aiming at lifting the static DAC mismatch errors in SAR conversion are presented. It will be shown that with these linearization techniques resolutions beyond 12 bits are achievable with a single SAR structure employing small capacitors.

2. SUB-BINARY SAR AND REDUNDANCY

A conventional SAR ADC employs a conversion algorithm termed binary search, in which the analog search range is halved in each successive bit-decision cycle. Exactly N steps are needed to resolve an N-bit word. The successive search ranges are usually set by a binary-weighted DAC which produces one analog level in each cycle to be compared with the sampled input. For example, during the MSB cycle the DAC produces a level corresponding to the code 10···0 or 01···1, one of the two codes closest to the midpoint of the ADC full scale V_{FS}. When the component matching of the DAC is ideal, the difference between these two codes is only one LSB, thus either choice yields no detectable difference to the ADC outcome. However, when mismatch is present the two choices will lead to drastically different results, which are better explained by the conversion curves illustrated in Fig. 1 for two scenarios. In the first case, the DAC MSB component is greater in value than the summation of all lower-rank components, resulting in two disjoint segments of the conversion curve (Fig. 1a). Since the analog input levels between the codes 01···1 and 10···0 all resolve to

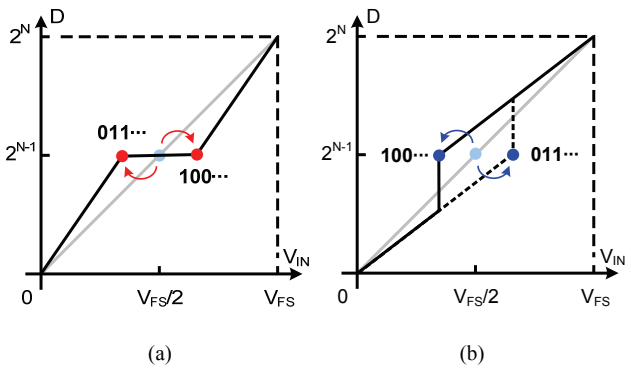


Fig. 1. SAR conversion curve due to MSB component mismatch: (a) super-binary and (b) sub-binary. The grey line indicates the ideal curve. V_{in} is the analog input and D is the raw decision vector ($D = \{d_i, i = 0…N-1\}$).

one digital LSB, the loss of information is irrecoverable from the digital domain alone. We term this scenario *super-binary*. The opposite case is shown in Fig. 1b, in which the analog levels corresponding to the codes 01···1 and 10···0 are swapped, resulting in an overlapped analog input range sandwiched by the two codes. We term this scenario *sub-binary*. Typically, depending on the pre-choice of the decision threshold, i.e., 01···1 or 10···0, during bit cycles, either the upper (solid) or lower (dashed) curve but not both will be exercised. The vertical discontinuity of the conversion curve thus leads to the absence of a chunk of digital levels termed missing codes.

A unique feature of the sub-binary conversion scheme is that if both the upper and lower segments within the overlapped range can be artificially enabled, any analog level inside this range can be mapped to two digital codes differing by the vertical distance between the two segments. We term this phenomenon *decision redundancy* or *architectural redundancy*. With a sub-binary architecture, it can be shown that the conversion nonlinearity due to missing codes can be fully corrected in digital domain under certain assumptions if the optimal bit weights are known [3],

$$V_{in} = V_R \sum_{i=0}^{N-1} \frac{C_i}{C_{tot}} (2d_i - 1) + QN, \qquad (1)$$

where V_{in} is the sampled input, V_R is the reference voltage, QN is the quantization noise, and the ratio of the i^{th} capacitor (C_i) to the total capacitance of the DAC (C_{tot}) defines the i^{th} bit weight w_i. Eq. (1) essentially guarantees that any two analog input levels at least one analog LSB apart will resolve to two distinct digital codes, or, equivalently, a digital-domain error correction is possible.

We note here that the sub-binary redundancy can be alternatively engineered using unit-element DAC by manipulating the SAR logic [1]. The binary-to-thermometer decoder required in a unit-element DAC is, however, undesirable due to its timing overhead and the extra logic needed to compute the redundant decision thresholds. A sub-binary DAC approach with hardcoded redundancy is preferred for high conversion speed [3], [8], [9]. Furthermore, the structure of a binary DAC can be retained while still providing redundancy by inserting additional decision steps into the binary search process periodically with some overhead to the SAR logic [2], [4]. Lastly, regardless of the exact redundancy form, bit-weight calibration according to Eq. (1) is dictated when random component mismatch is present, especially for a resolution of 10-bit and beyond. Section 3 will cover cases on how redundancy can be exploited to identify the bit weights.

3. DIGITAL BIT-WEIGHT CALIBRATION

3.1 Offset Double Conversion (ODC) [3]

This technique is derived from the superposition rule of linear systems. As shown in Fig. 2, a single SAR ADC digitizes each analog sample twice with two analog offsets, +Δ and –Δ, resulting in two raw codes, D_+ and D_-, respectively. Using identical bit weights, $W = \{w_i, i = 0, \cdots, N-1\}$, we first calculate the weighted sum of all bits for D_+ and D_-, denoted as d_+ and d_-, respectively. This actually realizes Eq. (1). The difference ε between d_+ and d_- is then obtained after removing 2δ (the digital version of Δ)—this difference should be ideally zero with optimal weights, guaranteed by the linearity of the ADC. A non-zero ε simply indicates incomplete learning of all bit weights and will direct the calibration to continue to adjust W until ε is driven to zero; at which point, the average of d_+ and d_- yields a proper digitization of V_{in}.

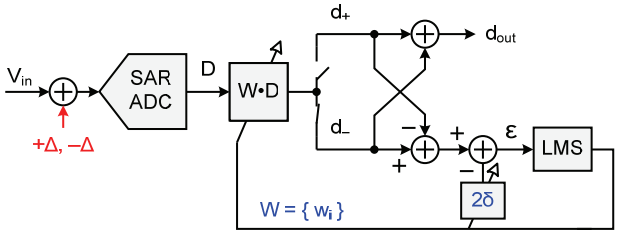
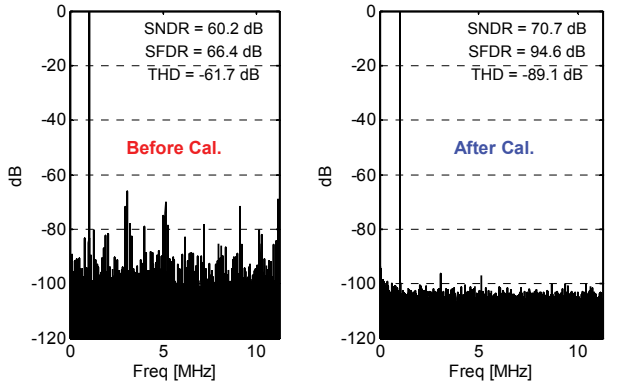


Fig. 2. ODC bit-weight calibration of SAR ADC



(a) (b)

Fig. 3. Measured output spectrum of a prototype 12-bit, 45-MS/s SAR ADC with ODC calibration: (a) before and (b) after calibration

The downside of ODC is that the conversion speed is halved in the background mode, while a benefit is that both the quantization noise and the comparator noise are attenuated by 3 dB in power due to averaging. The implementation of the offset injection is also very simple, i.e., one small capacitor and some digital logic. The convergence time of this technique compared to the correlation-based calibration [9], [10] is significantly shorter due to the deterministic and zero-forcing nature of the algorithm.

A prototype 12-bit SAR ADC was fabricated in a 1.2-V, 0.13-μm, 8M-1P CMOS process [3]. The active area of the ADC is 0.06 mm^2 and the total power consumption is 3.0 mW including calibration logic. The minimum capacitor size is set to 0.5 fF in this design. Driven by a 98% V_{FS}, 1.1-MHz sine wave at its input, the measured output power spectral density (PSD) of the prototype before and after calibration are shown in Fig. 3. With the calibration,

the SNDR, SFDR, THD were improved from 60.2, 66.4, 61.9 dB to 70.7, 94.6, 89.1 dB, respectively. The linearity improvement was nearly 30 dB. The convergence time was discovered to be inversely proportional to the magnitude of Δ—it takes about 22,000 samples to reach steady state when Δ is set to 25 LSBs.

3.2 Independent Component Analysis (ICA) [11]

Another SAR bit-weight calibration technique not subject to speed reduction is shown in Fig. 4, in which a pseudorandom bit sequence (PRBS) T of magnitude Δ is injected to the ADC input and gets digitized along with the analog input V_{in}. The digital output, obtained through a weighted sum of the individual bits of the raw digital output D, represents a digitization of $V_{in} + T{\cdot}\Delta$. If the ADC is ideal, the PRBS can be removed digitally, resulting in a digital output d_{out} (representing V_{in}) that is independent of T. When the optimal bit weights $W = \{w_i, i = 0, \cdots, N\text{-}1\}$ are unknown, the conversion process is nonlinear and the PRBS removal will be incomplete. Thus, the residual PRBS information in d_{out} can be exploited to infer the optimal bit weights.

A technical difficulty here is how to identify all N bit weights with the information of a single PRBS. Conventionally, estimating multiple model parameters dictates multiple PRBS injections, potentially degrading the ADC dynamic range and complicating the analog circuitry for injection. This is where ICA comes into picture [12]. As illustrated in Fig. 4, the technique operates on the bitwise correlation between T and the digital bits obtained through a digital re-quantizer, which mimics the SAR operation to decompose d_{out} back to its sub-binary format as D. This new digital output, termed $\hat{d}$, is correlated to T at bit level to direct the learning of all the bit weights. Since $\hat{d}_i$ and T are both one-bit signals, the digital logic implementing the correlation is simply an XOR gate.

A prototype 12-bit SAR ADC was fabricated in a 90-nm CMOS process [11]. The die area of the ADC is 0.05 mm^2. At 50 MS/s, the ADC consumes 3.3 mW from a 1.2-V supply. The PRBS injection is realized by one low-rank DAC capacitor at full sample rate. Fig. 5 presents the measured dynamic performance of the prototype. The calibration improves the SNDR and SFDR by more than 10 and 25 dB across the Nyquist band, respectively. The convergence time is around 10 million samples, or 0.2 seconds at 50 MS/s, with gear shifting applied to the LMS iterations.

3.3 Redundant Double Conversion (RDC)

The double conversion calibration illustrated in Fig. 2 can also be realized without explicit offset injection. Instead, the internal redundancy of a sub-binary SAR is exploited to facilitate the double conversion. As shown in Fig. 6, each sample is digitized twice, one using a sequence of decision thresholds corresponding to the DAC code 01···1 and the other 10···0. The effect of this, taking the MSB for example, is to create a bit-weight error detection window

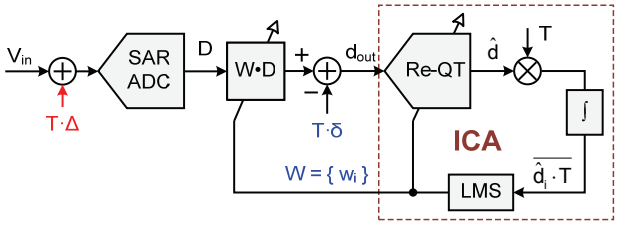


Fig. 4. ICA bit-weight calibration of SAR ADC

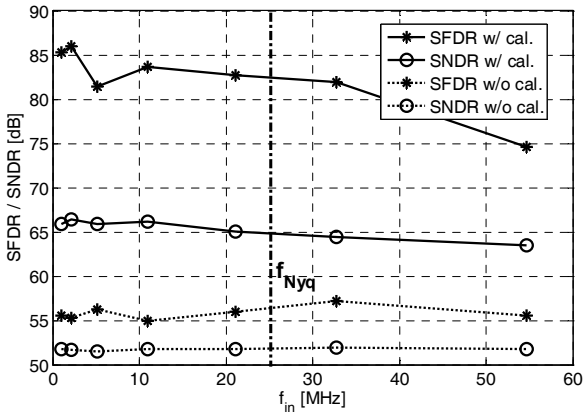


Fig. 5. Measured dynamic performance of a 90-nm, 12-bit, 50-MS/s SAR ADC prototype with ICA calibration

as large as the redundancy region shown in Fig. 1b. the two digitization outcomes d_+ and d_- are compared constantly for any difference—while a zero difference ε implies that either the bit weights are ideal or V_{in} is out of the redundancy region, a nonzero ε only means that the bit weights are not optimal and further adaptation is needed. All bit weights can be learned this way by altering the internal decision thresholds accordingly. Fig. 6 shows the two configurations in A and B, respectively.

RDC shares the same drawback of ODC, i.e., the ADC throughput is halved when operating in the background mode. However, there is no offset injection in RDC, thus there is no need to remove it digitally.

A prototype SAR ADC was fabricated in a 65-nm, 1.2-V CMOS process. The active area of the ADC is 0.05 mm^2. Fig. 5 shows the ADC output spectra before and after calibration for a full-scale 3-MHz sine-wave input. With the calibration, the SNDR and SFDR were improved from 30.0 and 31.4 dB to 71.4 and 94.1 dB, respectively. The LMS loop learns the optimal bit weights in less than 50,000 iterations, which is less than 3 μs with this ADC.

3.4 Internal Redundancy Dithering (IRD)

The 2× speed penalty associated with the RDC technique can be lifted if the shuffling of the internal configurations of A and B is controlled by a PRBS, leading to the fourth technique covered in this paper, the IRD. A system diagram of IRD is shown in Fig. 8, in which a back-end digital processor is employed to identify the MSB weight by correlating the corrected ADC output with the PRBS. Similar to the ICA case, to identify multiple bit weights,

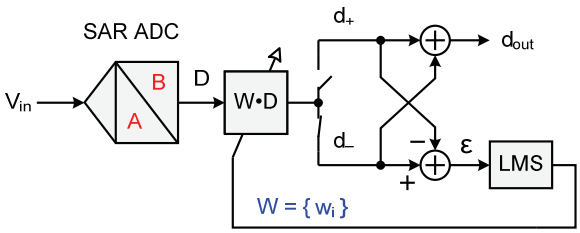


Fig. 6. RDC bit-weight calibration of SAR ADC. The labels A and B on the SAR symbol indicate that the bit-decision threshold corresponds to the DAC codes 01···1 and 10···0, respectively.

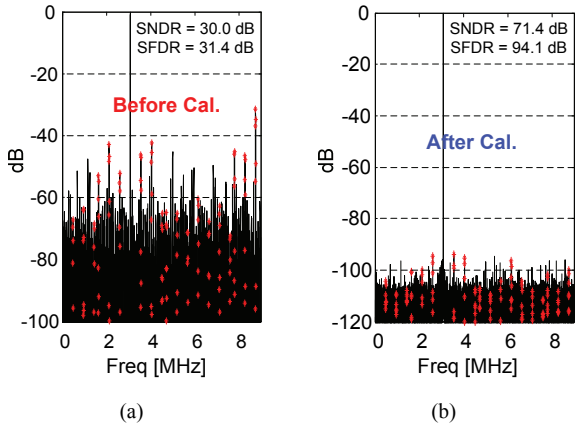


Fig. 7. Measured output spectrum of a prototype 65-nm, 12-bit, 36-MS/s SAR ADC with RDC calibration: (a) before and (b) after calibration

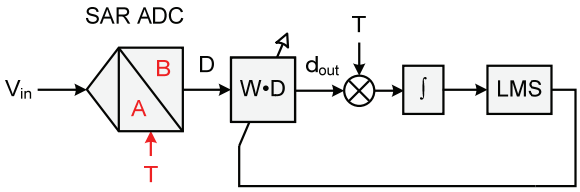


Fig. 8. IRD bit-weight calibration of SAR ADC. The labels A and B are defined the same as those of Fig. 6.

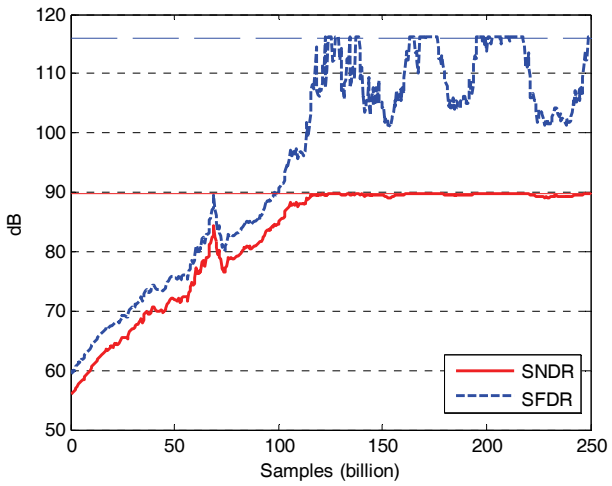


Fig. 9. Simulated learning curves of a SAR ADC employing the IRD bit-weight calibration technique

multiple correlations are required. In IRD, this implies that the PRBS responsible for decision threshold dithering will need to be different and uncorrelated for all the bits whose weights are to be identified. The convergence speed of the technique is expected to be slow due to the statistical fluctuation of the correlation process and the interaction between the learning loops of the multiple bit weights involved.

Fig. 9 illustrates the simulated SNDR and SFDR learning curves for the MSB learning case of a 15-bit SAR ADC. A significant linearity improvement of 30-40 dB is observed with calibration while the convergence time is 120 billion samples without gear shifting. The multi-bit case is currently under investigation.

4. CONCLUSION

Superior power efficiency and scalability continue to fuel the development of SAR converters in scaled technology. This paper reviews/presents a few techniques for digital background calibration of DAC bit-weight errors in SAR ADCs. With the dominant performance roadblock eliminated by calibration, SAR will become suitable and potentially dominate for broadband (100-200 MHz) and high-resolution (12-14 bits) applications such as wireless base-station and video streaming in advanced CMOS nodes.

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