Efficient Simulation of Continuous Time Digital Signal Processing RF Systems

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Abstract—A new simulation method for continuous time digital signal processing RF architectures is proposed. The approach is based on a discrete time representation of the input signal combined with a linear interpolation. Detailed theoretical calculations are presented, which prove the efficiency of the simulation when dealing with narrowband RF signals. We show that, when compared to a discrete time simulation, for the same simulation error, a decrease of almost two orders of magnitude is expected in the necessary number of input samples.
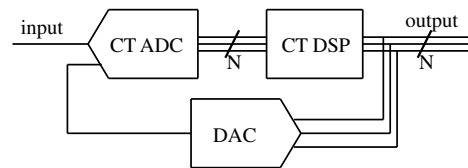
Fig. 1. Generic representation of a CT digital signal processing architecture. The system is composed of a CT ADC, a CT-DSP block and a DAC for feedback.

I. INTRODUCTION

Continuous time (CT) digital signal processing systems have been extensively studied over the past years. These systems rely on a continuous time level crossing (CT-ADC) analog to digital conversion stage followed by a continuous time digital signal processor (CT-DSP) block (Fig. 1). In some cases, the CT-DSP output is feedback to the input of the CT-ADC in order to enhance the performance of the conversion. One interesting property of these systems is that no quantization noise is observed because no quantization error is ever made. Furthermore, [1] shows that the data rate requirements are more relaxed as compared to those of synchronous systems. The CT design has been extensively deployed for low power, low frequency applications such as voice processing [2], fast control loops [3] and sensor interfacing [4].

With the recent advances in the deep submicron CMOS technologies, it has become possible to greatly increase the speed of the CT ADCs and of the CT-DSPs. The CT-ADCs have become good candidates for use in direct RF quantization architectures as they solve two important problems. First, the clockless design of these ADCs can greatly reduce the power consumption of the RF receiver. Second, their power consumption depends on input activity: when no input signal is present, the dynamic power consumption drops to 0. An RF implementation of a CT digital signal processing system has been presented in [5].

One of the remaining challenges in designing RF CT digital processing systems is efficient simulation. Fig. 1 presents a general representation of such a system. The simulation of the CT-DSP part can easily be done using an event driven approach, where level crossing events propagate from one system block to another with a certain behavioral and time delay model. However, the efficient generation of the level crossing events (referred to as timestamps) remains problematic since it is difficult to obtain a high precision on the time of the level crossings while using a fast simulator.

Analog simulation can be used for precise device level simulations, but it is too slow for architecture exploration needed to determine the specifications of the involved building blocks. On the other hand, discrete time simulation provides a fast and simple way of simulating CT digital signal processing architectures with a precision that depends on the ratio between the sampling frequency and the useful signal frequency (referred to as oversampling ratio - OSR). Since most of the current CT-DSP circuits are low frequency implementations, high OSR simulations are affordable. However, for RF implementations which operate at GHz frequency and require high frequency resolution, a brute increase of the OSR would greatly increase simulation time.

In this paper we present a hybrid simulation used for timestamp generation which attempts to minimize the simulation error while maintaining a low computational complexity. The rest of the article is organized as follows: Section 2 details the basic principles of the simulation; Section 3 provides a theoretical background for the simulation error computation for sinusoidal signals; Section 4 extends the validity of the results presented in Section 3 to general RF modulated signals. Section 5 applies these results to modulations used for IEEE 802.11a and IEEE 802.11b standards. The frequency representation of the error is discussed in Section 6. Lastly, Section 7 concludes the paper.
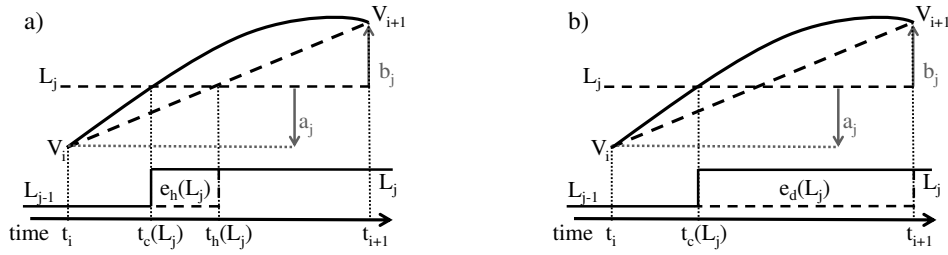
Fig. 2.   Level crossing error committed by the proposed hybrid simulation (a) and a discrete time simulation (b).

II. SIMULATION OVERVIEW

The basic principle used by the proposed hybrid simulation is presented in Fig. 2(a). Like the discrete time simulation (Fig. 2(b)), the proposed method uses a discrete time representation of the input signal but with a lower OSR. For each level crossing, a first order interpolation is used to determine the timestamp. In this case, the input signal crosses the level L_j and is sampled at time instants t_i and t_{i+1}. The interpolation produces the timestamp $t_h(L_j)$ which, in the case of RF signals, is a much better approximation of the real level crossing time $t_c(L_j)$ than the result of a synchronous simulation: t_{i+1}.

In order to compare the different simulation methods, performance metrics need to be defined. The two possible performance criteria would be simulation time and simulation error. Since this paper aims to provide readers with insight into architecture level simulations of CT digital signal processing RF systems, the analog simulation is not a good candidate because it is too slow and complex. For the rest of this article the hybrid and the discrete time simulations will be compared, while analytical calculations will be used as benchmark for precision. Finally, as an objective simulation time evaluation, the required OSR for each simulation will be compared for a given upper bound on the committed error.

We define the simulation error energy as the energy of the difference between a perfect CT signal and the respective simulation output. Considering a quantization step of q, the error energy for a level crossing is expressed in (1) for the hybrid simulation and in (2) for the discrete time simulation.

$$e_h(L_j) = q^2 \left| t_c(L_j) - t_h(L_j) \right| \quad (1)$$
$$e_d(L_j) = q^2 \left| t_c(L_j) - t_{i+1} \right| \quad (2)$$

Using this we can now define the signal to noise ratio (SNR) of the simulation as the ratio between the signal energy and the error energy. This expression will be used for performance evaluation for the rest of this article. For an input signal $V(t)$ of duration T which crosses levels L_1 to L_n we have that:

$$SNR = \frac{\int_0^T V(t)^2 \mathrm{d}t}{\sum\limits_{p=1}^{n} e(L_p)} \quad (3)$$

III. SINUSOIDAL INPUT

For a sinusoidal input in the form of $V(t) = A \sin(2\pi f t)$, the simulation error can be computed analytically for both simulation scenarios. As defined in Fig. 2, we have V_i and V_{i+1} the signal samples before and after the level crossing, $a_j = L_j - V_i$ and $b_j = V_{i+1} - L_j$. The error for a single level crossing as defined in (1), can be further developed as:

$$e_h(L_j) = q^2 \left| \frac{1}{2\pi f} \arcsin \frac{L_j}{A} - \left(t_i + a_j \frac{T_s}{V_{i+1} - V_i} \right) \right| \quad (4)$$

The difference between two consecutive samples (V_{i+1} and V_i) around the level L_j is approximated using a second order Taylor series:

$$V_{i+1} - V_i = \frac{2\pi}{OSR} \left(\sqrt{A^2 - (L_j - a_j)^2} - \pi \frac{L_j - a_j}{OSR} \right) \quad (5)$$

For simple input signals, precise expressions can be found for a_j, but since we require results which apply to more general cases, we opt for a statistical approach. In this case, a_j can be approximated as a uniform random variable bounded by the difference between two consecutive samples, as defined in (5). The resulting interval is expressed as follows:

$$-\frac{2\pi}{OSR} \left(\sqrt{A^2 - L_j^2} - \pi \frac{L_j}{OSR} \right) < a_j <$$
$$< \frac{2\pi}{OSR} \left(\sqrt{A^2 - L_j^2} - \pi \frac{L_j}{OSR} \right) \quad (6)$$

Finally, the error corresponding to each level crossing can be computed using the definition of the expected value of (4) given the specific distribution of a_j:

$$E[e_h(L_j)] = \int_{a_j} e_h(L_j) P(a_j) \mathrm{d}a_j \quad (7)$$

This integral is nontrivial, but can easily be computed numerically. By replacing this expression in (3) the theoretical value of the SNR can be computed.

Similarly, the discrete time simulation SNR can be computed using:

$$e_d(L_j) = q^2 \left| \frac{1}{2\pi f} \left(\arcsin \frac{L_j}{A} - \arcsin \frac{L_j + b_j}{A} \right) \right| \quad (8)$$

By symmetry, b_j is a uniform random variable defined over the same interval as a_j (6).

These theoretical calculations are compared with simulation results. For a given number of bits, we plot the corresponding SNR obtained from the hybrid and the discrete time simulation as well as the values predicted by the theory. Using a sinusoid quantized over 5 bits, we plot the results in Fig. 3. Similarly,
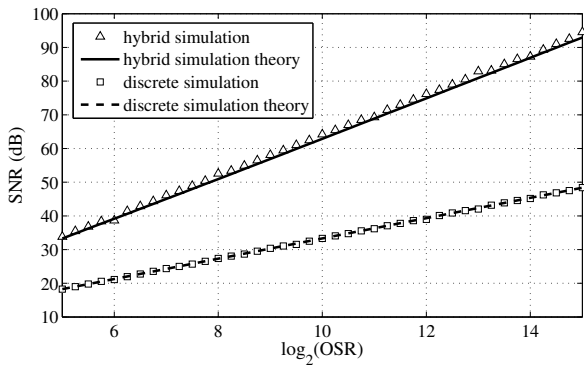
Fig. 3.   SNR versus the OSR for the hybrid and discrete time simulation using a single sinusoidal input quantized over 5 bits.
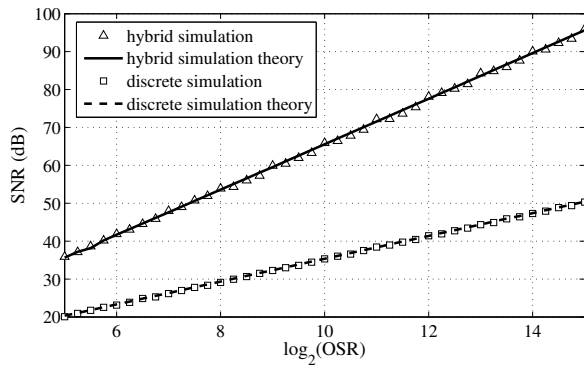

Fig. 5.   SNR versus the OSR for the hybrid and discrete time simulation for an amplitude and phase modulated sine quantized over 5 bits.
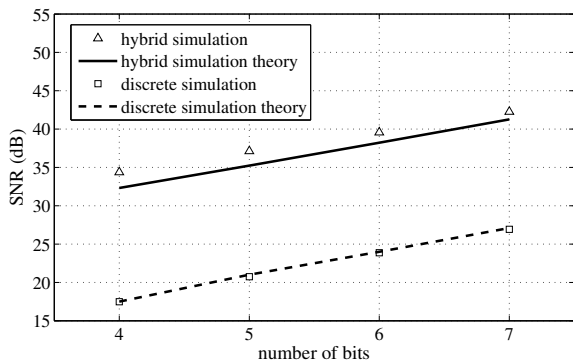

Fig. 4.   SNR versus the number of bits for the hybrid and discrete time simulation using a single sinusoidal input oversampled by a factor of 64.

Fig. 4 shows the evolution of the simulation error versus the number of bits for an OSR of 64.

As we can see, the theoretical results are closely matched by the simulation. The maximum difference is only about 2dB and comes from the approximations related to the linearization of the sine function over small intervals. Moreover, there is a significant gain in using the hybrid simulation as opposed to the discrete time simulation. For a given SNR of, for example 50 dB, a reduction of a factor greater than 2^7 is expected in the representation of the input signal. The corresponding speedup gain of the hybrid simulation will be slightly less than 2^7 because extra interpolation points need to be computed.

IV. SIMPLE MODULATED SIGNALS

In this section we will extend the previously derived results to a more general case. An RF signal can be represented as a sine wave carrier with phase and amplitude modulation:

$$V(t) = A(t)sin(2\pi ft + \phi(t)) \qquad (9)$$

By supposing that $A(t)$ and $\phi(t)$ vary slowly with respect to the sinusoid and by following the same procedure as before, the error committed by the hybrid simulation for each level

crossing L_j can be derived:

$$e_h(L_j) = q^2 \left| \frac{1}{2\pi f} \arcsin \frac{L_j}{A(t_i)} - \left(t_i + a_j \frac{T_s}{V_{i+1} - V_i} \right) \right| \qquad (10)$$

As in the previous case, a_j can be defined as a uniform random variable. Its interval of variation can be derived from (6) by replacing the old constant amplitude value (A) with the new time varying amplitude defined in (9), equal to $A(t)$.

It is interesting to note that the phase component $\phi(t)$ completely cancels out in the error expression (10). This result can be easily interpreted by the slow variation of $\phi(t)$ with respect to the sinusoid. At any given time t, the phase is expected to remain constant for at least one period of the sinusoid, which is equivalent to a phase shifted version of the signal used in the previous section. Since the previously derived results do not depend on the initial phase of the signal, it follows that the simulation error for modulated signals is only determined by the amplitude modulation term $A(t)$.

In order to compare the theoretical results with a simulation, simple analytical expressions have been chosen for $A(t)$ and $\phi(t)$ so that the true level crossing times can be computed: $A(t) = k_1 t$ and $\phi(t) = k_2 t$. As in the previous case, we use a 5 bit quantizer. k_1 is chosen so that the amplitude modulation term varies from 0 to full scale over 32 periods of the carrier sinusoid. The phase modulation constant k_2 is chosen so that the phase varies from 0 to 2π over the same number of carrier periods. The results are shown in the Fig. 5.

Once again we see a very good agreement between the simulation and the theory. The proposed hybrid simulation greatly decreases the OSR required for a given SNR. More importantly, the results in this section prove that the previously derived formulae can be used to compute the expected value of the simulation error for any narrowband RF signal, as long as its discrete time baseband representation is known.

V. GENERAL MODULATED SIGNALS

In this section we will study the simulation performance for IEEE 802.11a and IEEE 802.11b signals. The signals are
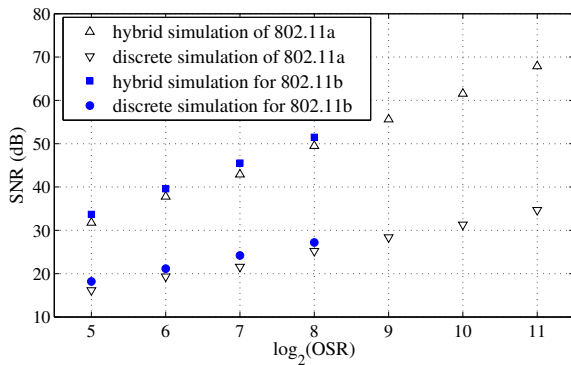
Fig. 6. SNR versus OSR for two wireless standards: 802.11a and 802.11b using the proposed hybrid simulation as well as a discrete time simulation

Fig. 7. Total SNR and band limited SNR versus the OSR for a sinusoidal input using the proposed hybrid simulation and the discrete time simulation

quantized over 5 bits and the results using the previously derived theory are plotted in Fig. 6. Since both standards have similar baseband amplitude distributions, the obtained SNRs are also very similar. Furthermore, the use of the hybrid simulation drastically reduces the necessary discrete time representation of the input signal for a given error limit. At 40 dB precision, a hybrid simulation only requires an input OSR of 64 instead of 4096 required by the discrete time simulation.

VI. ERROR IN THE FREQUENCY DOMAIN

Until now the total absolute error introduced by the simulation has been derived. However, when dealing with RF signals, it is interesting to study the repartition of this simulation error over the frequency spectrum. Since most RF signals use different frequency bands, in order to provide a fair comparison, the simulation error will be integrated between 0 Hz and the maximum useful frequency contained in the input signal.

For white noise, an SNR gain of the form $20 \log \frac{BW}{F_s}$ would be expected, but this is not be the case. The error, as expressed earlier, is the difference between the simulation output and a perfect level crossing version of it. However, as it has been shown in [6], a level crossing signal has frequency components which contain the fundamental frequency, as well as all of its harmonics with no noise in-between. By limiting the bandwidth of our signal, we will be cutting off high frequency noise as well as parts of our signal - more specifically - its harmonics.

In this section we will consider a sinusoidal input signal at 1 GHz frequency, quantized over 4 bits. The band limited simulation error is compared to the total error for both the hybrid and the discrete time simulation in the Fig. 7. Before analyzing the results, it is important to note that a non-uniform discrete time Fourier transform (NDFT) has been used, since the samples from the hybrid simulation are not periodic. A classic DFT would have required to synchronously resample the asynchronous output of the hybrid simulation which would have introduced another error component.
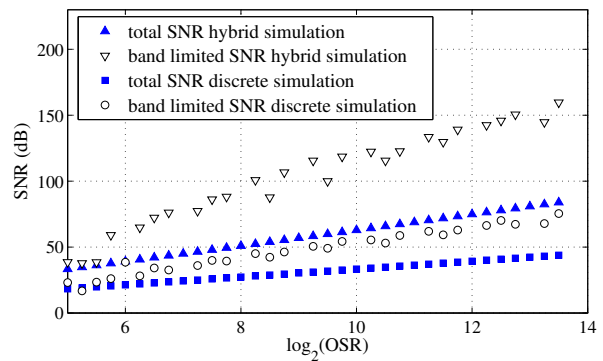
The band limited results show an even higher gain in precision for the hybrid simulation compared to the discrete time simulation. Using the proposed hybrid simulation, 50dB SNRs can be expected using input OSRs as low as 32.

VII. CONCLUSION

In this paper we have presented a detailed account of the error introduced by a new simulation method for CT digital signal processing RF systems. The proposed method combines the discrete time and the continuous time approaches by using an oversampled version of the input signal and a first degree interpolation in order to enhance the precision of the level crossing times. It has been shown that the proposed simulation greatly decreases the simulation time when compared to a purely discrete time approach. Moreover, the expressions derived in this paper enable the computation of the simulation error prior to the actual simulation for any RF signal which has a known baseband representation.

The proposed simulation method has been successfully used to study the tradeoffs for the building block parameters used in two CT digital signal processing RF architectures.

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