APPLIED MATHEMATICS FOR THE MODELING OF A NON-LINEAR SOI COMPLEX DEVICE

Cristian RAVARIU

"Politehnica" University of Bucharest – Faculty of Electronics Telecommunications and Information Technology,
Splaiul Independentei 313, 060042, Bucharest, Romania
cristir@mcma.pub.ro

ABSTRACT

The active electron device modelling is a reference section inside the non-linear systems. Among the SOI transistors, the pseudo-MOS/SOI can be achieved on any SOI wafer, being a test device. Being an active component, this transistor provides strong non-linear characteristics. The pseudo-MOS transistor presents a higher complexity versus the classical MOSFET: using a proper back-gate bias an inversion channel occurs through the bottom of the SOI film and the device work as un up-side down MOSFET; the accumulation channel also provide a MOSFET-like behaviour; also a depletion regime allows the non-linear electrical conduction thru the neutral channel. The previous models are relied on the depletion approximation since to compute the potential and electric field distribution. The advantage is the simplicity; but they can be applied just for depletion regime. This paper computes exact solutions of the Poisson's equations, solved on the pseudo-MOS geometry and offers an accurate model of the electric field and potential along the SOI structure, in all regimes of work. The analytical models are accompanied by ATLAS simulations.

Keywords: *Non-linear systems, SOI, active devices.*

1. INTRODUCTION

The SOI (Silicon On Insulator) nowadays technology offers a large spectrum of integrated non-linear micro-systems: SOI-MEMS for biological handling [1], solar cells, [2], or advanced signal processing, [3].

In a previous work, the electric field and potential distributions were computed, in the depletion approximation, for a pseudo-MOS transistor, [4]. This device is commanded by the back gate. These models are simple and accurate just for small gate biases, so that the strong inversion or accumulation is avoided. Therefore the previous models introduce considerable errors when the device works in strong inversion, for instance.

The channels charge neglecting was reflected in a threshold voltage underestimation. This is encountered especially in the SOI devices with channels on both sides of the buried insulator. The SIMOX technology provides n film on p substrate, with smaller doping concentrations in the substrate. When the inversion conditions in the film occur, the substrate is already in strong inversion [5]. Taking into account the channels electric charges imposes in this case.

The goal of this paper is to solve the Poisson's equation in non-depletion approximation for a pseudo-MOS transistor. The results will be used to establish a more accurate analytical model for the threshold voltage, which will be compared with the previous one. The analytical models have to be accompanied by ATLAS simulations. This new model is necessary for the accurate electrical characterization of the pseudo-MOS transistors that frequently work in the strong inversion regime.

2. THE EQUATIONS CAPTURING

The analysis is focused on a partially-depleted SOI pseudo-MOS transistor, with n film and p substrate, without electric charge in the buried insulator.

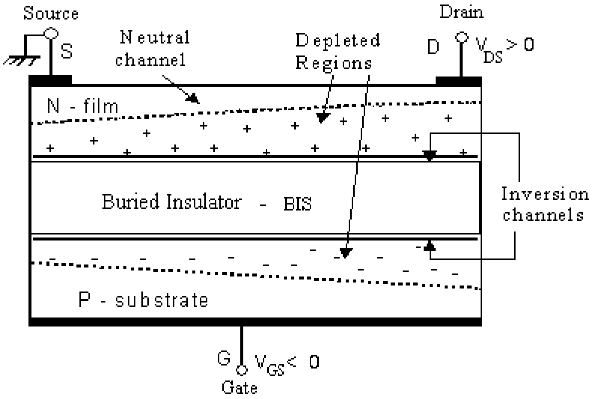


Figure 1: *The analyzed pseudo-MOS transistor.*

Figure 1 presents the transistor with the source and drain on the top of the film and the gate on the bottom of the structure. The notations are: $x_{S1/2}$ – the film/substrate thickness, x_{BIS} – the BIS thickness, $x_{d1/2}$ – the space charge region extension in the film/substrate, $\Phi_{F1,2}$ – Fermi potentials in the film/substrate, $N_{D,A}$ – the doping concentrations in the film/substrate, $\varepsilon_{Si,\ BIS}$ – dielectric permittivity of the Si/BIS, n_i – intrinsic concentration, $\alpha=q/kT$ – a notation, Φ – the potential, x – distance, V_G, V_S, V_D, - the voltages of the Gate, Source, Drain. A negative gate bias is necessary to invert the n – type film, fig. 2. The Poisson's equation can be written:

In film, $x\in(0,x_2)$

$$\frac{d^2\Phi}{dx^2} = -\frac{qn_i}{\varepsilon_{si}}\left[e^{-\alpha(\Phi+\Phi_{F1})} - e^{\alpha(\Phi+\Phi_{F1})} + e^{\alpha\Phi_{F1}}\right]. \quad (1)$$

In substrate $x \in (x_3, x_5)$

$$\frac{d^2\Phi}{dx^2} = -\frac{qn_i}{\varepsilon_{si}}\left[e^{\alpha(-\Phi+V_G+\Phi_{F2})} - e^{\alpha(\Phi-V_G-\Phi_{F2})} - e^{\alpha\Phi_{F2}}\right]. \quad (2)$$

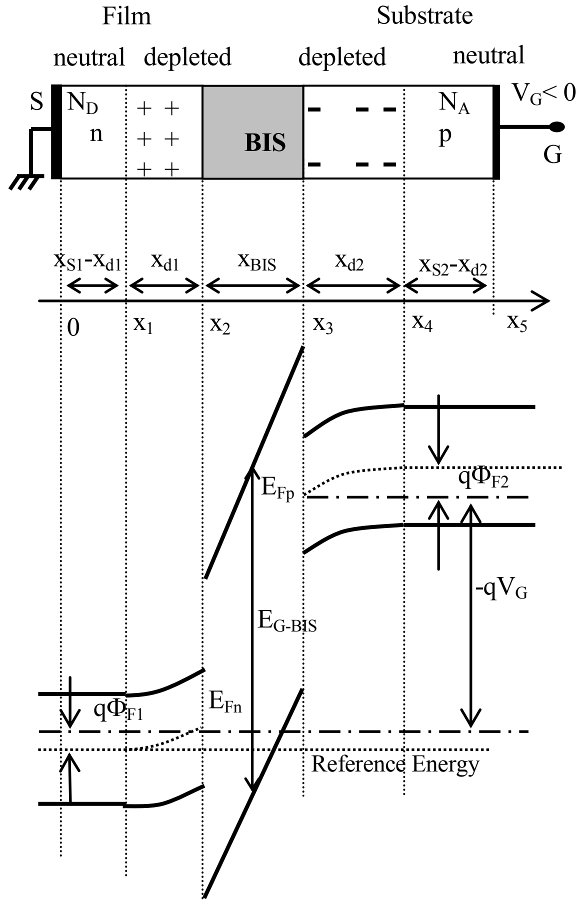


Figure 2: *A cross-section through the previous structure, between source and gate. Beyond the structure, the energetic diagram is available.*

The limit conditions for neutral contacts are:

In film:

$$E(0)=0,\ \Phi(0)=V_S=0\,. \quad (3)$$

In substrate:

$$E(x_5)=0,\ \Phi(x_5)=V_G\,. \quad (4)$$

After first integration operation of the Poisson's equations, the following expressions of the electric field versus the potential results:

In film, $x \in (0, x_2)$

$$E(\Phi) = \sqrt{\frac{2qN_D}{\alpha\varepsilon_{si}}}\begin{bmatrix}\left(e^{-\beta\Phi} - e^{-\beta V_S}\right)e^{-2\alpha\Phi_{F1}} + \\ + \left(e^{\alpha\Phi} - e^{\alpha V_S}\right) - \alpha(\Phi - V_S)\end{bmatrix}^{1/2}. \quad (5)$$

In substrate, $x \in (x_3, x_5)$

$$E(V) = \sqrt{\frac{2qN_A}{\beta\varepsilon_{si}}}\begin{bmatrix}\left(e^{\beta(V-V_G-2\Phi_{F2})} - e^{-2\beta\Phi_{F2}}\right) + \\ + \left(e^{\beta(V_G-V)} - 1\right) + \beta(V - V_G)\end{bmatrix}^{1/2}. \quad (6)$$

where $E_{Fp,n}$ = quasi-Fermi levels for holes/electrons, $E_{G\text{-}BIS}$ – the buried insulator band gap. Because the buried insulator doesn't contain electric charges, the following relationship between the interfaces potentials: $\Phi(x_2) = \Phi_{S1}$ and $\Phi(x_3) = \Phi_{S2}$, yields:

$$\Phi_{S1} = \Phi_{S2} + \frac{\varepsilon_{Si}}{\varepsilon_{BIS}} E_{BIS} \cdot x_{BIS}\,. \quad (7)$$

where E_{BIS} is the constant electric field from the buried insulator. From the conservation of the normal electric induction component at both interfaces of BIS, the electric fields $E(x_2)= E(\Phi=\Phi_{S1})$, $E(x_3) = E(\Phi=\Phi_{S2})$ are equals because:

$$E(x_2) = E(x_3) = \frac{\varepsilon_{Si}}{\varepsilon_{BIS}} E_{BIS}\,. \quad (8)$$

Replacing (8) in (5), (6), a new relationship between Φ_{S1}, Φ_{S2} is obtained:

$$\begin{aligned}&N_D\left[\left(e^{-\alpha\Phi_{S1}} - e^{-\alpha V_S}\right)e^{-2\alpha\Phi_{F1}} + \left(e^{\alpha\Phi_{S1}} - e^{\alpha V_S}\right) - \alpha(\Phi_{S1} - V_s)\right] = \\ &= N_A\left[\left(e^{\alpha(V_{GS}-\Phi_{S2})} - 1\right) + \left(e^{\alpha(\Phi_{S2}-V_{GS})} - 1\right)e^{-2\alpha\Phi_{F2}} + \alpha(\Phi_{S2} - V_{GS})\right]\end{aligned}. \quad (9)$$

3. AN ACCURATE MODEL FOR THE THRESHOLD VOLTAGE

Usually source is grounded (V_s=0). Starting from the standard definition of the threshold voltage of a pseudo-MOS/SOI transistor: Φ=-2Φ_{F1}, and replacing it in the equations (7), (9), a system with the variables: Φ_{S2} and V_G (that is V_T now), results. Solving this system, the threshold voltage is the unknown of the following equation:

$$\begin{aligned}&\left(\frac{N_D}{N_A}\right)^2 2\alpha\Phi_{F1} + 1 = \\ &= \exp\left(-2\alpha\Phi_{F1} - 2\alpha\Phi_{F2} - \frac{\alpha}{C_{BIS}}\sqrt{2qN_D\varepsilon_{si}\cdot 2\Phi_{F1}} - \alpha V_T\right) - \\ &- \alpha\left(2\Phi_{F1} + \frac{\sqrt{2qN_D\varepsilon_{si}\cdot 2\Phi_{F1}}}{C_{BIS}} + V_T\right)\end{aligned}. \quad (10)$$

It is important to notice, that the surface substrate potential, Φ_{S2}, is generally treated, not particularized like in the previous models. If the exponential term is neglected in (10), that correspond to the electric charges neglecting in the channels and supposing additionally that the surface substrate potentials is Φ_{S2}=-2Φ_{F2}, the general expression (10) becomes the simplified model, [6]:

$$V_T = -2\Phi_{F1} - \frac{1}{C_{BIS}} \cdot \sqrt{2\varepsilon_{Si} q N_D} \cdot \sqrt{2\Phi_{F1} - 2\Phi_{F2}} \, . \quad (11)$$

The relation between the exact model (10) proposed here and the old simplified model (11), is analyzed in the discussion paragraph, resulting systematically higher errors when the old model is used.

4. SIMULATIONS AND COMPARISONS

The analytical models are compared with numerical simulations made with ATLAS software. The simulated SOI structure had: x_{S1}=1,5μm; x_{S2}=2μm; x_{BIS}=0,4μm; BIS=oxide; N_D=10^{15}/5x10^{15}/10^{16}cm^{-3}, N_A=10^{14}/10^{15}cm^{-3}.

The threshold voltages were computed by three methods:
(1) ATLAS simulations;
(2) The exact model - the equation (10);
(3) The simplified model - the equation (11).

The ATLAS simulations revealed an interesting behavior. Even for neutral contacts, a distribution of potential still exists at zero biasing (V_G=V_S=V_D=0V). Figure 3 presents in a cross-section between source and gate, the potential drops over the structure. The source is grounded, but the film potential is +0.32V. The gate is grounded, but the substrate potential is –0.288V. The reason consists in the Fermi levels misalignment from film and substrate due to their different doping (5x10^{15}cm^{-3} in n-type film and 10^{15}cm^{-3} in p-type substrate typically for a real SIMOX process).

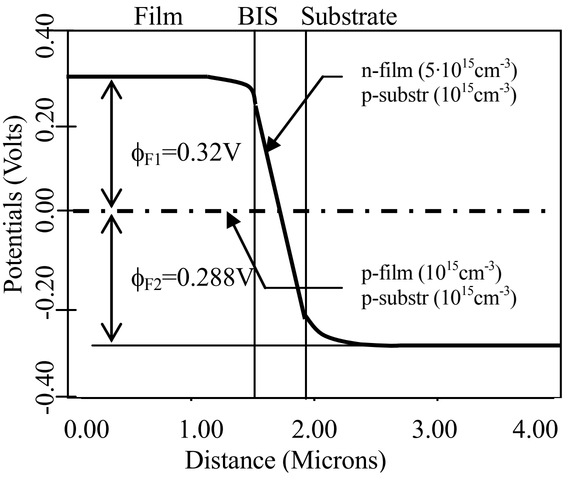


Figure 3: *The potential distribution between Source and Gate in a pseudo-MOS transistor with:* x_{S1}=1.5μm, x_{S2}=2μm, x_{BIS}=0.4μm, V_G=V_S=V_D=0V, *after ATLAS running.*

When the film and substrate are putting together, via Source and Gate terminals at zero voltage, the relaxation of Fermi levels implies a transfer of carriers (like in a pn junction); consequently, constant Fermi levels occur, followed by a band bending. So, the potential drop over film and substrate becomes:

$$\Phi_{np} = \frac{1}{\alpha} \ln \frac{N_A N_D}{n_i^2} = 0.32 - (-0.288) = 0.608V \, . \quad (12)$$

That corresponds to the above doping concentrations. If the film and substrate have the same type and the same doping, no potential drop over the structure occurs at zero biases, as is shown in figure 3 after ATLAS running.

The external Gate – Source voltage is superposed over the internal potential difference. Hence, the analytical model of the threshold voltage must be corrected by the potential Φ_{np}.

Figure 4 presents the extraction methodology of the threshold voltage by ATLAS simulations for different doping concentrations in film and substrate. The gate voltage was increased up to the potential bending becomes $2\Phi_{F1}$ in film.

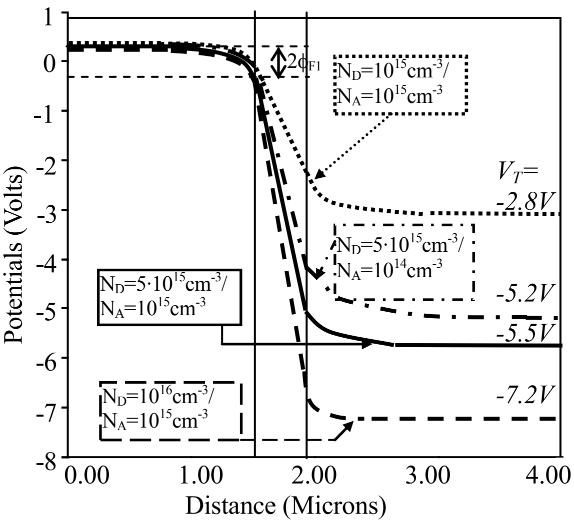


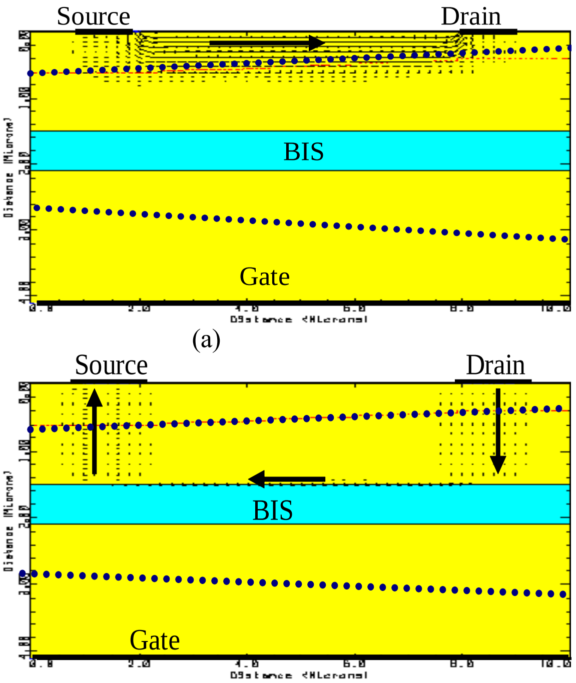
Figure 4: *The potential distributions between Source and Gate in the pseudo-MOS transistor, at different conditions.*

At the right side of the figure 4 is emphasized the threshold voltage value extracted with ATLAS.

Figure 5 proves the device complexity during the work conditions. The simulation shows the global current flow between source and drain with little current vectors. An enrich electrons conduction from the left to the right side occurs through the neutral channel from the film surface, fig. 5.a, and a poor holes inversion current thru the film bottom occurs from the right to the left side, fig. 5.b. The arrows illustrate the flow sense for carriers.

When the gate voltage becomes so negative, so the depletion is limited and the inversion channel still arises, the main sub-component of the pseudo-MOS transistor enter in action - the MOSFET, back-gate commanded, [7].

At this point, the pseudo-MOS transistor fulfils its election function: a dedicated device for the SOI interfaces characterization, using the inversion current thru the film bottom.



(a)

(b)

Figure 5: *The current flow vectors in a partially depleted pseudo-MOS transistor with: (a) neutral channel and (b) an inversion channel at the film bottom.*

5. DISCUSSIONS

A comparison among exact model (10), simple model (11) and reference Atlas model is available in table 1. Here are focused the main results of the simulations and the analytical models of the threshold voltage, V_T and the error, *Er*., versus the Atlas simulations. The doping concentrations N_A, N_D are varied in order to observe the models accuracy.

Table 1: *Data comparisons.*

N_A = [cm^{-3}] **N_D = [cm^{-3}]**	**10^{15}** **10^{15}**	**5 x 10^{15}** **10^{14}**	**5x10^{15}** **10^{15}**	**10^{16}** **10^{15}**
V_T Atlas [V]	-2.8	-5.2	-5.5	-7.2
V_T Exact [V]	-2.77	-5.24	-5.34	-7.08
V_T Simple [V]	-2.75	-4.96	-5.08	-6.85
Er. Exact [%]	1.07	0.76	2.90	1.66
Er.Simple [%]	1.78	4.61	7.63	3.24

As expected, the threshold voltage increases with the doping concentrations. The optimum error is encountered for that doping concentrations in film and substrate that ensures a simultaneously inversion onset. The errors of both analytical models were computed in respect with ATLAS simulations. The final averages relative errors are: for exact model – *Er*=1.60%, and for simplified model – *Er*=4.32%. The simpler model (11) brings a 7.63% maximum error and the accurate model (10) brings a 2.9% maximum error. The accuracy of the model (10) increases for that values of the doping concentration that ensure a simultaneously inversion onset at film bottom and substrate surface. The presented model (10), based on exact solutions of Poisson equation gives the minimum errors, for all cases, as is shown in the table 1.

6. CONCLUSIONS

A new model for the threshold voltage, based on the exact solutions of the Poisson's equation, was derived. In respect with the ATLAS simulations, the new exact model provides a better fitting than the old simplified model, (the average relative error decreases from 4.32% for old model up to 1.60% for new model). The disadvantage of the new model is the non-linear equation that must be solved. But this model is more suitable for thin and ultra – thin insulator layers. The old model is suitable for that constructive data that allow roughly a simultaneously inversion conditions at both buried insulator interfaces. However, the quick solution of the old model can be used to start the iterations for the threshold voltage exact extraction with the new model.

ACKNOWLEDGMENTS:

This work has been co-funded by the Financial Agreement POSDRU/89/1.5/S/**62557** and PNII **- 12095, 62063**.

REFERENCES

[1] C. Ravariu, L. G. Alecu, A. Bondarciuc, F. Babarada, Advanced SOI semiconductor structures for micro-dose biological samples handling, *Journal of Opto-electronics and Advanced Materials - Rapid Communications*, vol. 4, nr. 9, Sept., 2010, pp. 1375-1378.

[2] S. Burtescu, C. Parvulescu, F. Babarada, E. Manea, The Low Cost Multicrystalline Silicon Solar Cells, *Journal Mat. Science and Engineering B: Advanced Functional Solid-State Mat.*, vol. 165, no. 3, pp. 190-193, 2009.

[3] D.N. Vizireanu, Quantized Sine Signals Estimation Algorithm for Portable DSP based Instrumentation, *International Journal of Electronics, Taylor & Francis*, Vol. 96, Issue 11, Nov. 2009 , pages 1175 – 1181.

[4] C. Ravariu, A. Rusu, F. Ravariu, Parameters extraction from some experimental static characteristics of a pseudo-MOS transistor, Bucharest, *UPB Scientific Bulletin*, Series C, vol. 70, no. 1, pp. 29-34, 2008.

[5] S. Sato, K. Komiya, N. Bresson, Y. Omura, S. Cristoloveanu, Possible influence of the Schottky contacts on the characteristics of ultrathin SOI pseudo-MOS transistors, *IEEE Transactions on Electron Devices*, Aug. 2005, Volume : 52, Issue:8 , pp. 1807.

[6] S. Cristoloveanu, Sheng S. Li, *Electrical characterization of silicon-on-insulator materials and devices*, Kluwer Academic Publishers, New York, 1995.

[7] X. Luo, D. Fu, L. Lei, B. Zhang, Z. Li, S. Hu, Z. Zhang, Z. Feng, B. Yan, Eliminating Back-Gate Bias Effects in a Novel SOI High-Voltage Device Structure, *IEEE Transactions on Electron Devices*, 2009, vol. 56, no. 8, pp. 1659-1666.