Full-Chip Analog Circuit Simulation in a Multi-core and Cloud Environment

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As the number of transistors integrated on a chip keeps growing exponentially, so does the need for more simulation and verification provided by Electronic Design Automation (EDA) tools. Today, the opportunity does not come from speedier processors as the clock rate of processors has leveled off and does not follow the continuing increase in the speed (cut-off frequency) of tinier transistors, but from multi-core processors and cloud computing.

The focus of this presentation is on the growing need for full-chip electrical simulation of analog and mixed-signal Integrated Circuits (ICs) and the opportunities offered by parallel compute environments.

The potential productivity gains in IC design using the industry-standard SPICE simulator on parallel state-of-the-art hardware are going to be presented based on a detailed analysis of the SPICE solution. The two main components of SPICE and its run time, semiconductor device model evaluation/linearization and linear-equation solution, and the potential for their parallelization will be described.

The challenge is adapting existing proven algorithms that are sequential in nature, to parallel architectures. The best efforts in this area remain subject to Amdahl's law, implying that even cutting 90% of the execution time by parallelization, only a speedup of one order of magnitude can be achieved. Therefore, application programs adapted to parallel architectures can profit from no more than a small number of processors, usually eight. However, for designs relying on optimization and statistical computation where multiple solutions need to be computed independently of each other, the speedup scales almost linearly with the number of processors available.

Examples of typical large circuits that require most accurate solutions provided by SPICE and the speedups obtained on multi-core computers are presented. For speedups beyond what can be obtained through parallelization, a new class of simulators, FastSPICE, based on a gradual user-controlled relaxation of the SPICE algorithm accuracy, will be described briefly.