Dual frequency comprehensive transponder with inverse load modulation

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***Abstract* – Today's passive RFID tags are designed and constructed for one frequency band and optimized for maximum performance. But many applications in transportation and identification could profit from the benefits of two- or multi-resonant systems and could deliver enhanced solutions. This article shows a new concept for a dual power system functional at EPC HF and EPC UHF RFID band with only one common antenna and two antenna pads. A typical high performance RFID system contains a well tuned resonance circuit with a high quality factor. At the maximum field strength or maximum radiated power, the excessive power delivered to the chip could cause damage to the inlay. Inverted load modulation is presented in this paper to handle this temperature problem. As a UHF performance limitation it should be considered that a standard 120nm FLASH-CMOS process without Schottky - diode option is used.**

I. Introduction

Heating up of the chip

RFID-TAG manufactures will typically try to achieve good energy and communication performances. In far operation range applications, the focus will be to tune the Tag's resonance-tank as precise as possible to the dedicated system frequency. In UHF systems power matching between Tag coil and chip will insure that the maximal received power is delivered to the chip. Also in HF Tags with accurate impedance matching and small resistive losses are essential and will result in a high quality factor. The resonance frequency of the matching circuit should be exactly at 13.56MHz measured and tuned at weak field-strength. For example in ISO14443 systems, RFID-chips used in passport applications consume more than 10mW DC power. Such high performance systems use a coil with small inductance which will cause also small inductor impedance. These power optimized Tags will convert at high field-strengths (10A/m) most of the received energy into temperature. This problem gets with each design innovation step or technology-shrink more serious because chip area will be reduced but the surrounding conditions like maximum ambient temperature, field strength or radiated power will keep constant. To limit the temperature especially in the inductive coupled case of a HF transponder a new load modulation concept and voltage limiter will be presented.

Multi frequency TAG

In logistic and identification typically one frequency domain is used. If a dual or even a multi frequency antenna is used and the chip is able to handle the different bands, many new applications could benefit by preferring on band. Why multi band solutions are not manufactured and pushed by companies up to now? One reason is that single frequency chips are smaller and cheaper. Furthermore is the resonance circuit of such an Inlay easier to tune to it's resonance frequency and once again it will cost less (especially when single side UHF coils are used). Also the coil shape and total area could be chosen more flexible in single frequency RFID solutions.

To keep competitive with multi frequency systems compared to single frequency solutions, it is important to increase the cost of the antenna and chip only moderate and try to keep the contactless performance comparable with narrowband systems.

II. Detailed Implementation

There are several methods to reduce the chip temperature in HF but also in UHF configuration. In both systems a resonance circuit is used to convert the radiated power from the interrogator to electrical power for the chip. A frequency sweep of the antenna coil voltage U_2 in Figure 1 shows the response of a simplified parallel resonance circuit. The center frequency of 13.56MHz is primarily independent of the parallel resistor R_{shunt} which will limit the coil voltage to a defined value. The current through the shunt resistor will stay constant in the first approach.

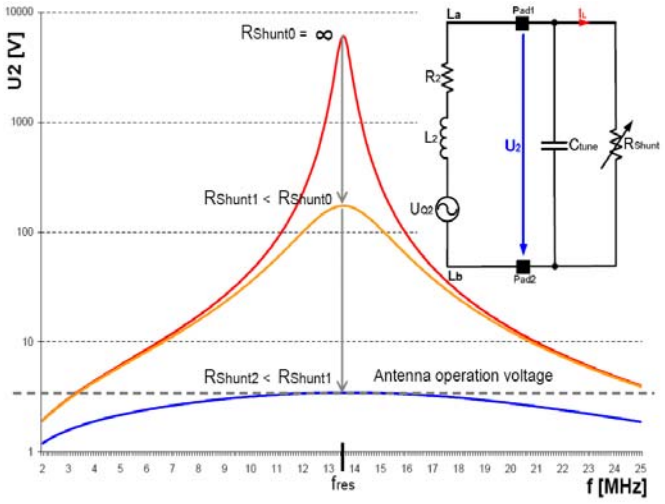

FIGURE 1 – TRANSPONDER PARALLEL RESONANCE CIRCUIT

The coil voltage U_2 could also be limited by tuning the chip capacitance to a higher value. But this will result in a considerable increase of chip area in HF systems.

The relation between the basic resonance tank components and the coil voltage U_2 is:

$$U_2 = \frac{U_{Q2}}{1 + (j\omega L_2 + R_2)\ \ (1/R_{Shunt} + j\omega C_{tune})} \qquad [1]$$

The chip temperature is finally proportional to the dissipated power in the shunt regulator which is furthermore proportional to the coil voltage U_2.

Architecture of the analog frontend

The shunt transistor is a part of the regulation loop and implemented with NMOS transistor between the coil contact pads, which will limit U_2. This voltage value will be a few hundred mV above one threshold voltage, where the chip can still be powered. A charge pump is necessary to reach an internal power supply voltage level of VDD internal of about 1.5V. Figure 2 shows the architecture of the power path front end.

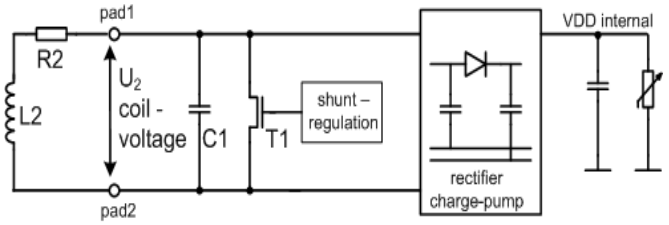

FIGURE 2 - ARCHITECTURE OF THE POWER FRONTEND

The shunt circuit limits the coil voltage to a minimum value, where the charge pump is working with optimum efficiency. Additionally the shunt transistor can also act as a load modulator in the inverse or in the traditional load modulation mode [6,9,10].

Conservative and inverse load modulation

During TxD the load modulator varies the chip input resistance by increasing the gate-source voltage of transistor T1. With this traditional concept the generated sideband voltages according ISO10373 will be below the limits, because the coil voltage difference during load modulation is not sufficient. Inverse load modulation [2] can solve this problem and will generate a big enough sideband voltage also at weak field-strengths. During release of the chip load the coil voltage will rise up to a defined maximum voltage level. If it is reached, the shunt transistor T1 will act once again as limiter. One additional benefit of the inverse load modulation is a dramatically reduced oxide-stress time of the transistors which are attached to the coil. This can once again help to increase the sideband voltage. Figure 3 shows the nominal coil voltage starting in idle operation condition at about 1V peak and rises up during modulation to 7V. The field-strength at this test was set to 300mA/m and measured under nominal conditions.

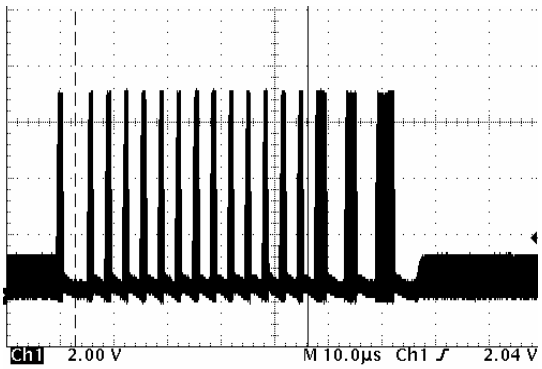

FIGURE 3 - INVERSE LOAD MODULATION
(EPC HF CODING USED)

With this analog frontend design concept also the traditional concept can be applied. During load modulation the input resistance of the chip is reduced and the coil-voltage will decrease. In this case the advantage of chip temperature reduction and relaxed oxide reliability are gone. Furthermore the regulation loop of the shunt circuit has to be fast and precise in the minimum voltage level. If the coil voltage swing is too small the clock recovery module will miss some cycles, the timing is wrong and the side band frequency out of specification.

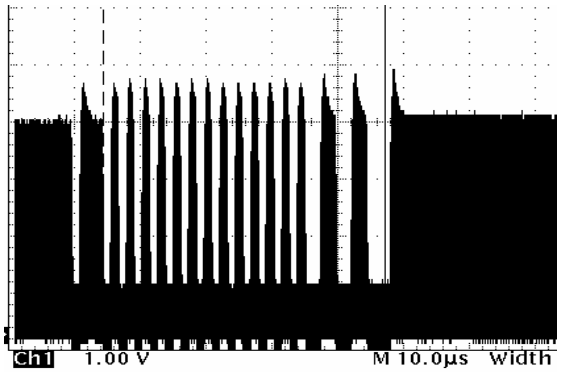

FIGURE 4 - CONVENTIONAL LOAD MODULATION
(EPC HF CODING USED)

Both modulation concepts could be applied to a multi frequency chip but to reach a good UHF performance too, some important design topic should be considered. At high frequencies (above 800MHz) and low power at the antenna (below -10dBm) the coil voltage level is smaller than the threshold voltage of medium voltage MOS transistors.

To archive the maximum voltage at the rectifier, the chip input capacitance and radiation resistance should as small as possible. U_2 is the input peak voltage, $P_{pad1,2}$ the power at the chip, R_2 is the radiation resistor and C_{chip} the input capacitance. Following equation is valid for power matching:

$$U_2 \approx \sqrt{\frac{P_{pad12}}{R_2}}\ \ \frac{1}{\omega C_{chip}} \qquad [3]$$

A small C_{chip} capacitance could be the reason to take the conservative load modulation concept. In HF mode the coil voltage will be regulated to 4V and a shunt transistor with a small transistor-width is still be able to reduce it's resistance during load modulation thanks to the high Ugs voltage of about 4V. Finally the system integrator of the application has to choose the modulation type. In UHF mode backscattering is done by applying high Ugs voltages to short the shunt transistor. A UHF reader is much more sensitive than former HF reader and does not need the big dynamic in the coil voltage changes at the chip.

The multi frequency rectifier and DC/DC converter

This new power supply concept can support energy from LF up to 2.45GHz. Figure 4 shows the architecture of the power supply path. Only one configurable rectifier is used and delivers power for analog modules and the digital part. The silicon area overhead for the selective mode configuration is small (about 20% of the power rectifier).

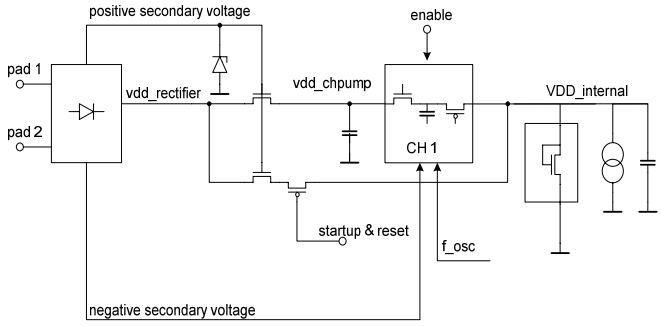

FIGURE 5 - POWER GENERATION WITH RECTIFIER, SERIAL-REGULATOR AND CHARGE PUMP

During startup the module responsible for the frequency detection and selection is not powered and cannot deliver the right information to the rectifier. So a uniform startup condition is necessary where the most important modules are powered up. In Figure 6 a typical transient coil voltage waveform is shown. Weak field strength of 80mA/m is applied to the 13.56MHz resonant system and the rectifier starts in the uniform mode which is similar to the UHF mode. After a small overshoot, the coil voltage settles at about 1.8V. Before the power on reset releases, the rectifier is switched in its HF mode and the voltages rise up after a certain time to 3.5V. If the tag is powered in UHF mode, the coil voltage is not switched and the rectifier will stay in its initial state.

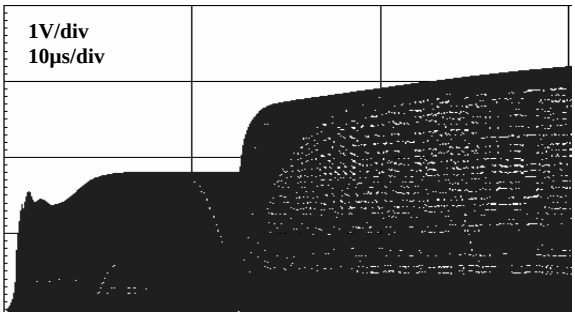

FIGURE 6 - POWER GENERATION WITH RECTIFIER, SERIAL-REGULATOR AND CHARGE PUMP

In UHF mode so called secondary supplies are generated. They are generated with weak charge pumps and so the loaded current at these supplies is small.

After the rectifier, two NMOS transistors are attached acting as DC/DC converter. The gate voltage for these high side regulators is delivered by one of the secondary supplies from the rectifier. Also the serial regulator will start via the lower NMOS transistor and the PMOS transistor. In HF mode this PMOS is low resistive too and will deliver power for the internal VDD. If a UHF carrier is applied the PMOS transistor is witched off and the charge pump serial to the upper NMOS transistor will be enabled. To block high voltages in HF mode generated at the output of the rectifier the NMOS serial regulator in front of the pump is needed. For UHF only RFID tag the charge pump could be connected to the rectifier and would generate the internal VDD with a higher efficiency.

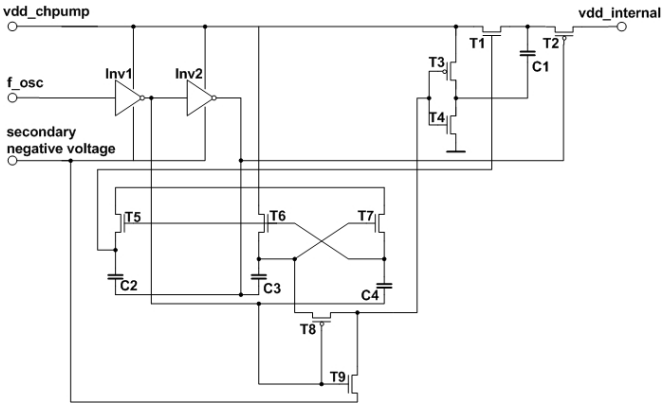

FIGURE 7 - DETAILED SCHEMATIC OF THE LOW VOLTGE CHARGE PUMP

To reach a high efficiency in UHF mode, it is important for the charge pump to double the voltage already at a very low supply voltage. Also in the inverse load modulation mode it will help to reach bigger sideband voltages, when the pump works already at low voltages. The negative secondary supply helps to reach a minimum power supply voltage of 500mV for the voltage doubler. In normal operation mode and during the low voltage phases of load modulation the serial regulator will deliver 0.7V and the charge-pump will push it to about 1.5V. A local oscillator delivers the f_osc clock frequency of 2.5MHz ± 15%. This oscillator is anyway necessary to satisfy the requirements of the EPC global class-1 gen-2 UHF RFID specifications [4] and is connected to the f_osc node of the charge pump which is buffered with two drivers already connected to the negative supply node. During the low phase of f_osc the power path transistor PMOS T2 is conducting well and will deliver charge from C1 to the energy reservoir capacitor VDD. At the clock high phase an additional voltage doubler charge pump will push the gate of the NMOS T1 to a high potential and the capacitor C1 is charged again.

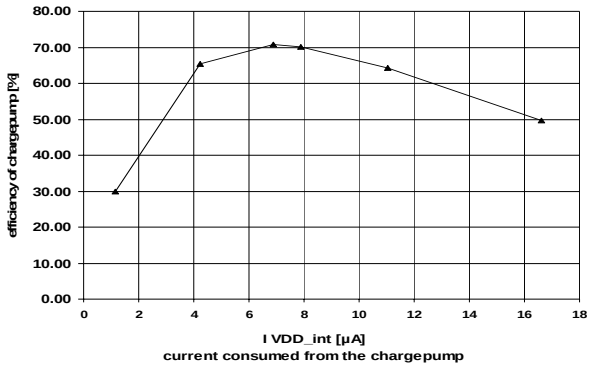

FIGURE 8 - EFFICIENCY OF THE CHARGE PUMP VERSUS CURRENT CONSUPTION

Fig 8 shows the efficiency of the charge pump at a power supply voltage of 550mV. In memory-read mode a peak-current is consumed by the whole chip system and will reach approximately 8µA. The component dimensions of the pump are fitted to reach the highest efficiency at this point of 71%.

III. CONCLUSION

We have developed an analog frontend for multi frequency band RFID tags. A new flexible and high efficient power supply concept was introduced which could be used for singe frequency band tags too. Simulations and first measurements have shown that the energy-performance of this architecture is competitive compared to single HF systems. To handle the big voltage dynamic from 7V close to 0V, transistors with an increased oxide-thickness and length are used. Area overhead limitation was achieved by reusing modules for each frequency band.

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