Enhanced Demodulator Implementation for Mobile Satellite Internet Systems

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Abstract—In this paper, we implement the robust demodulator for mobile broadband satellite internet access systems. Especially, in order to achieve the good synchronization under very low SNR, a large frequency offset, and Doppler frequency offset with constraints of mobile satellite communication, we introduce the efficient carrier freq. offset estimating algorithm and the carrier phase estimating algorithm collaborate with the channel decoder of a Turbo coded modulation for mobile DVB-RCS system. The proposed techniques can fulfill the stringent up-link link budgets at Ka band by operating at very low SNR.

Keywords-component; formatting; **Very Low SNR, TDMA Burst, Joint carrier recovery and channel decoding**

I. INTRODUCTION

Satellite communication systems are generally enlarged for having an good downlink capacity. However, recently more and more applications like interactive television/internet, demand an uplink channel from the terminal via the satellite to the provider's gateway (e.g. the DVB-RCS standard)[1]. Since these terminals have antennas with small diameters, the SNR remains relatively rather low. In addition, at high frequencies (in particular, at Ka-band), RF power amplifiers are major cost factors for the user terminal. Therefore, there is a strong interest in developing power-efficient solutions to facilitate the deployment of interactive multimedia systems in the consumer market where the user terminal cost is of principal factor.

Hence, strong error correcting codes, like Turbo Codes, need to be applied in low SNR environment. The weakness of turbo code is that they require almost ideal carrier synchronization at the receiver. In current designs of burst-mode demodulators for DVB-RCS, synchronization has been proven to be one of the major limitations on the achievable performance. This fact manifests itself in particular at low code rates, where the channel signal- to-noise ratio (Es/No) is also low.

The DVB-RCS standard provides preceding training data before each data burst, so called preamble, used by the receiver to estimate the channel parameters. As this preamble diminishes the energy and transmission efficiency of the transmission by reducing the amount of employed data symbols, it is kept rather short. With this short preamble, the receiver is not able to adequately track dynamic channel parameters. Thus, in order to iteratively reduce the estimation errors, it is possible to re-use the soft information provided by the decoder. In this paper, we introduce the carrier phase estimating algorithm to be integrated into the channel decoder of a turbo coded modulation for mobile DVB-RCS system. And, we developed the improved carrier freq. offset/Doppler estimating algorithm to facilitate the H/W implementation. The paper is organized as follows. Section II defines the system model and section III refers the algorithm-centered design of demodulator, respectively. Design feature of the algorithms developed in section III is evaluated in terms of the BER performance in section IV. Finally, Section V presents some conclusions

II. SYSTEM MODEL

We assume that the uplink of a satellite system, from a mobile user to the satellite[1], could maintain LOS condition and we consider the demodulator operates on AWGN or Ricean fading channel. In this paper, we only regard the link environment as AWGN with very low SNR by exploiting active array antenna. To optimize the system capacity in mobile environment, burst mode is generally considered as TDMA access scheme. The complex envelop of the sampled received signal is given by

$$r(kT_s) = \sum_n a_n g(kT_s - nT - \varepsilon_o T) e^{j(2\pi\Delta f T_s + \theta_o)} + n(kT_s) \qquad (1)$$

where, a_n is a sequence of MPSK data symbol, $g(t)$ is the impulse response of the convolution of the transmitted pulse with channel impulse response and matched filter, T is the symbol duration, and $T_s = T/4$ is a sampling time., $n(kT_s)$, Δf and $\Delta\theta$ indicates a complex-valued AWGN, a frequency offset, and initial phase offset, respectively

III. DESIGN OF DEMODULATOR

Synchronization is obtained at the following process: timing recovery, carrier frequency recovery and phase recovery.

A. *Symbol Timing Estimator*

Various schemes for feedforward symbol timing estimation have been presented, which were identified by their nonlinear functions; Square-Law Nonlinear (SLN) [2][3], Absolute Value Nonlinear (AVN) [4], and Log Nonlinear(LOGN) [5]. They require sampling rate of 4 times symbol rate. If the jitter performance and H/W complexity should be considered, it would be more suitable to design the symbol timing estimator as the AVN algorithm. The estimate of the timing error $\hat{\tau}_k$ as eq. (2), is used to control the interpolator and decimation unit and is computed once at the beginning of each transmission block.

$$\hat{\tau}_k = -\frac{T_s}{2\pi}\arg\left\{\sum_{k=1}^{4L}\left|r\left(\frac{kT}{4}\right)\right| e^{-jk\pi/2}\right\} \qquad (2)$$

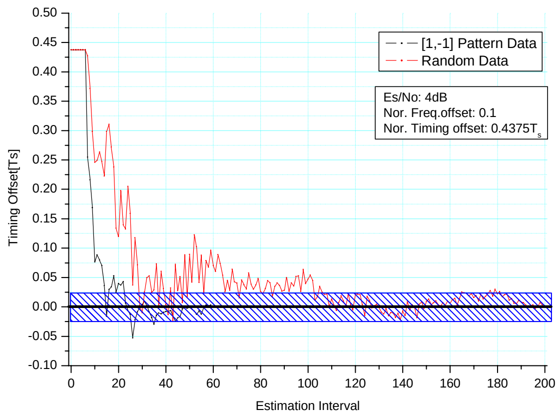

Figure 2. Acquisition performance of the AVN timing estimator

where, L indicates the length of the estimation symbol. The AVN algorithm could be implemented by digital circuit as eq.(2), properly. The acquisition time of symbol timing error is shown in fig. 2 and we can acquire reasonable results by setting the estimation interval (L) as 30 symbols with specific data pattern in fig. 2. Figure 3 indicates that the AVN algorithm shows enhanced performance in jitter variance compared with commonly used the O&M algorithm [3].

B. *Interpolator for timing control*

After estimating the time error, in the units subsequent to the Interpolator, we can use only one sample per symbol obtained at the optimum time instant. To design the proper interpolator, we investigate the common interpolation techniques for timing adjustment in [6, chap. 9]. The interpolator will produce the sequence

$$y_n = \sum_{i=-2}^{1} C_i(\mu_n)\cdot x[(l_n - i)T_s] \qquad (3)$$

$$l_n = \mathrm{int}(t_n / T_s), \mu_n = t_n / T_s - l_n$$

where, the coefficients $C_i(\mu_n)$ are polynomial FIR interpolator due to its favorable implementation structure in μ_n. Polynomial coefficients are tabulated in [6, pp. 521--523]. l_n is called the basepoint index and μ_n the fractional interval.

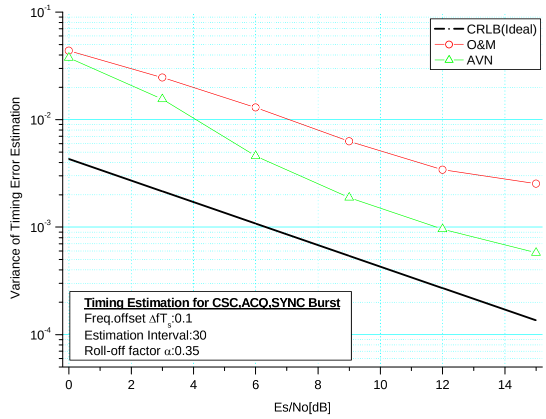

Figure 3. Jitter performance for various timing estimator algorithms

C. *Unique Word Detector*

Unique word sequence w_k should have good property of aperiodic autocorrelation defined as

$$C(\tau_{UW}) = \sum_{k=1}^{L_{UW}-\tau_{UW}} w_k w^*_{k+\tau_{UW}} \qquad (4)$$

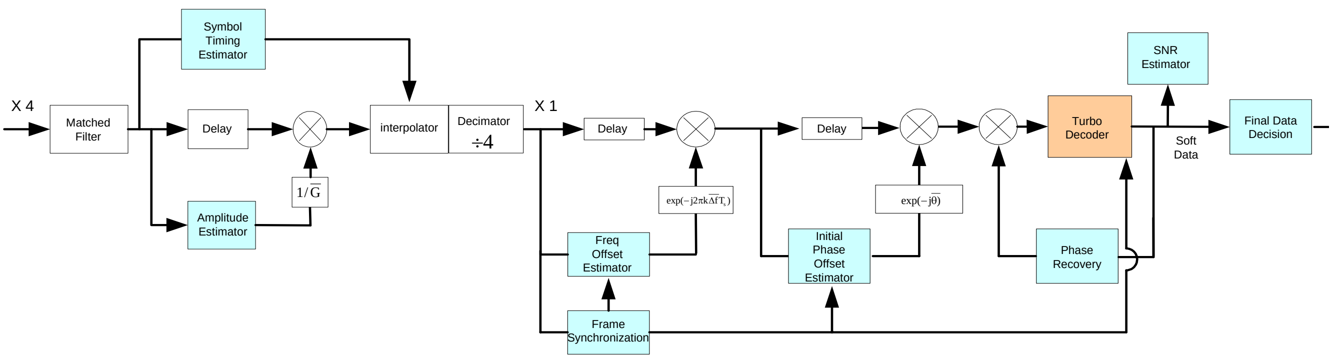

Figure 1. Demodulator Structure

where, L_{UW} is the unique word (UW) length in symbols and τ_{UW} is the delay between the received sequence and the correlator's sequence in the detector. The best sequence for this purpose is Barker sequence, with which it holds that $|C(\tau_{UW})|\leq 1$ for $\tau_{UW}\neq 0$. Maximal length of known binary and quaternary Barker sequences is 13. However, that value is too short to use for detecting frame of signals transmitted through poor satellite channel environment. Accordingly, we consider binary *m*-sequence as UW sequence, which seems to have small aperiodic autocorrelation when τ_{UW} is restricted within small values. In this paper, we introduce differential PSK UW detector like [6] (pp. 487) working well under large freq. offset, and its performance is analyzed in [7], perfectly. Decision variable F^{DPSK} is given by

$$F^{DPSK} = \left| \sum_{k=1}^{L_{UW}^{DPSK}} z_k w_k^* \right|^2, \quad z_k = x_k x_{k-1}^* \tag{5}$$

where L_{UW}^{DPSK} is the length of the differentially decoded UW and x_k is the received complex symbol. Mobile terminal transmits the differentially encoded UW of length $L_{UW}^{DPSK}+1$. By detecting the UW, we can carry out the frame synchronization.

D. Carrier Freq. offset Estimator

Frequency offset estimators based on data-aided (DA) for TDMA burst MODEM, have been presented [8-10]. L&R scheme [9] has good performance with low complexity but smaller estimation range as the number of correlator length(N) increases. By using the method proposed by M&M [10] considered to be the most promising, as complexity increases, the improved estimation performance can be obtained while maintaining the estimation range unchanged. It has a rather stringent requirement in terms of H/W implementation at the expanse of increased acquisition range. Therefore, in order to achieve the good synchronization under large carrier freq./Doppler offset (Practically, it is required to estimate the initial normalized freq. offset by about 10% when the initial access burst would try to access the network offset) and reduce the H/W complexity, we introduce modified DA frequency estimator with a moving average technique in fig. 4.

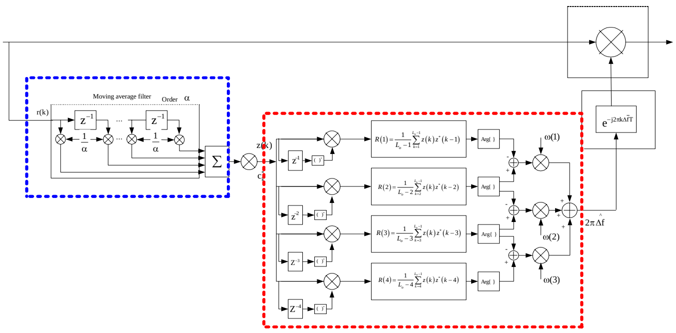

Figure 4. Modified DA(Data-Aided) carrier freq./Doppler offset estimator with moving average filter

It can improve the jitter performance without increasing the estimation interval as feedforward structure at the cost of narrowed estimation range as increasing the tap length of moving average filter. Therefore, we can achieve the carrier freq. recovery as M&M with moving average filter tap length 10 and reduce the variance of jitter without a large implementation burden in fig. 5 and fig. 6. For specific example, we can achieve the same effect of 8 correlators by applying to 4 correlators with MAF tap 6. Therefore, we can reduce the computational complexity by 50% with considering the reasonable lock range. The specific numerical comparison about it relatively would be described in following table.

Table 1. Computational load as the preamble length(Lo:64) and the number of correlator(N) (Data-Aided operation)

Algorithm	Real Products & Additions	Total Sum
M&M [8]	$N(2L_o - N - 1)/2$	3814
M&M with MAF tap 6	$N(L_o - N - 1)/2$	1978

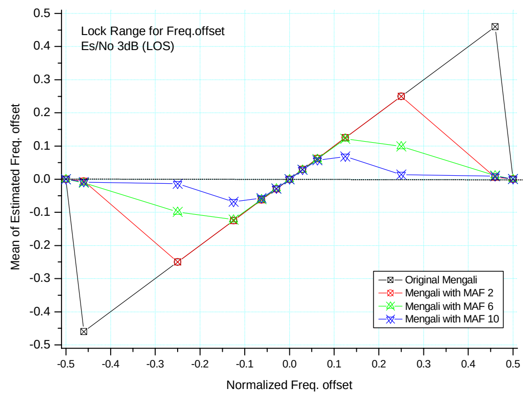

Figure 5. Expectation of $\overline{f_d}T$ vesus f_dT with modified M&M algorithm

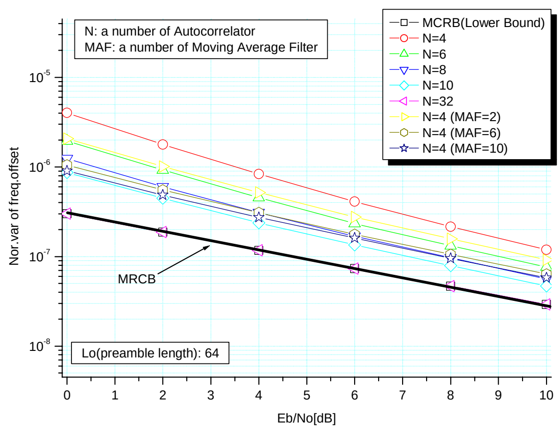

Figure 6. Accuracy of M&M algorithm with MAF as following the tap length

E. *Coarse Carrier Phase Offset Estimator*

For a carrier phase recovery, classical syhchronization algorithms lead to a large amount of jitter and numerous cycle slips in low SNR environment. To minimize the performance degradation by initial phase offset and the to facilitate the operation of iterative decoding at the joint carrier phase recovery and decoding block, it would be in need of removing the initial phase offset. It's required to use inevitable premble symbols with short length to remove the residual frequency offset and phase offset, roughly. The use of the preamble allows DA operation and results in superior performance in comparison with NDA scheme in very low SNR. In this paper a sliding window feedforward phase estimator based on the Viterbi & Viterbi(V&V) algorithm is adopted for initial operation mode[11]. To avoid biased estimation, only the estimate associated with the symbol centered on the sliding window is used. This estimator is used in the first iteration to compensate for the absence of decoder output. The window size is considered as an even number L of the total preamble length. Therefore the known symbols $\{d_i^{'}\}$ the same as the sliding window length are used to obtain the DA estimate

$$\bar{\theta}_{DA}(n) = \arg\left\{ \sum_{i=\max[0,k-L/2]}^{N_{pre}-1} r_i e^{-j\Delta\bar{f}nT} d_i^{'} \right\} \tag{6}$$

In figure 7, the channel encoder block diagram is depicted. The turbo encoder, composed of two recursive systematic convolutional (RSC) encoders and an interleaver, has code rate r =1/2 and constraint length ν =4. The information bit sequence $\{d_k\}$ is organized in packets of length N and feeds the turbo encoder producing the systematic sequence $\{x_k^s\}$, and the parity check sequence $\{x_k^{1p}\}$ $\{x_k^{2p}\}$. In the turbo encoder, the puncturing block is introduced to reduce the effective encoder rate to r=1/2.

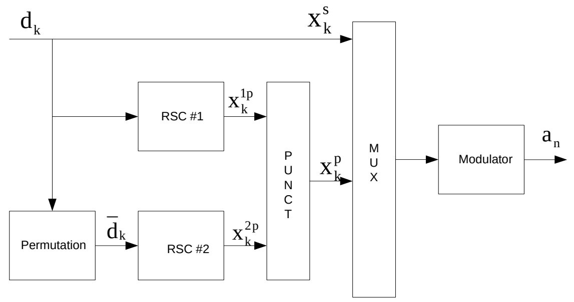

Figure 7. Transmitter block diagram

Phase recovery is implemented iteratively using the APP(a posteriori probability) reliability given by the turbo decoder. This iterative technique gives advantages with respective to a hard feedback, since more reliable information improves the phase estimator performance. After the decoding process, the soft input data of second decoder, for all transmitted symbols can be exploited for phase estimation. The simplest idea is to adopt the ML formular weighted by data reliability drive the phase estimator more than the less reliable ones. The iterative decoding procedure is based on a modified BCJR algorithm for simpler H/W implementation. At the first iteration step, decoder #1 outputs the log a posteriori probability ratio(LAPPR) for the general n-th information bit μ_n in the data block under decoding, given as follows

$$L(\mu_n) = \log\left(\frac{P_r\{\mu_n = 1 \mid r\}}{P_r\{\mu_n = -1 \mid r\}} \right) \tag{7}$$

The carrier recovery block based on LAPPR value, works with iterative decoding, takes advantage of the progressive reliability improvement inherent in iterative decoding, and above all comes to a improved carrier estimate at the end of the iterative process. However, this estimator has a fatal weak point of performance degradation when it would have input values with residual freq. offset and a large of initial phase offset. Therefore, in order to overcome it, we introduced the initial carrier phase estimator function at section III-E, but we could not remove the residual freq. offset, perfectly. Additionally, it is required to compensate the residual freq. offset. We design the simple freq. estimator within decoding process

$$FD(\overline{\Delta f}) = \arg\left\{ \sum_{n=0}^{N-d-1} r(n+d)r(n)^{*} \right\} \tag{8}$$

Where, N is burst length and d is the symbol interval for estimation. As the number of iteration increases, the LAPPR can have reliable value by updating likelihood function. Despite of this process, it can not acquire the reliable data while compensating residual freq. offset. Therefore, we should update the LAPPR value after freq. offset compensator operates, perfectly. If we apply to this concept at 1 ATM transmission, we can achieve the desired performance through small iteration. By introducing this idea, we can anticipate about SNR gain of 0.25dB at BER = 3×10^{-3} in figure 8.

F. *Implementation Results*

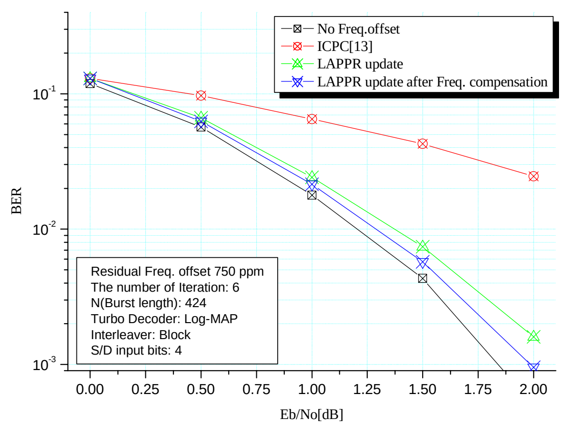

Figure 8. BER performance of demodulator

We achieve the enhanced receiver H/W implementation related with algorithms proposed in section III and construct the analog IF(Intermediate Frequency) loop back test environment. Detailed information is described in Table 2. The performance of the implemented modem that incorporate the proposed schemes are compared with that of the system with a conventional scheme[13]. The proposed algorithm can provide the performance improvement by 1dB compared to the conventional scheme as shown in figure 8. In figure 9, it shows the configuration for demodulator test connected analog circuit for IF loop back. The demodulator board is shown in figure 10. The main FPGA device consists of two Xilinx Virtex II 8000 chips, one 1000 chip for demodulation algorithm and decoder, PLX 9054 chip for PCI I/F(interface), an oscillator and some interface chips for other modules.

Table 2. Specification for demodulator H/W test

Item	Specification
Channel Bandwidth	6.144 MHz
IF Freq. Range	6.912 MHz ~7.68MHz
Freq. Selection	1Hz steps
Preamble	For Removing large freq. offset and initial phase offset
Decoding	Turbo (Log-MAP),.r=1/2
Burst Type	1 ATM (N=412)
Descrambler	DVB-RCS compliant
Interface	Ethernet, PCI Interface
Command/Control	Serial RS-232

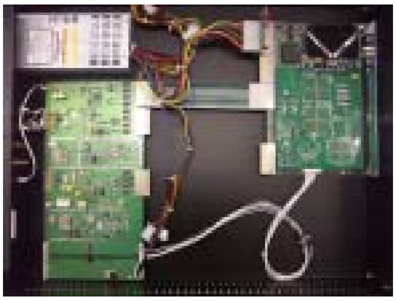

Figure 9. Demodulator test for analog I/F Board

IV. CONCLUSION

In this paper, we have implemented the robust demodulator for Mobile Broadband Satellite Internet Access System at very low SNR channel. Taking advantages of the moving average filter with small jitter and joint carrier recovery/decoding, the proposed algorithms are able to cope with very low SNR as well as large freq. offsets. Although all results shown in this paper are for the AWGN channel, first trials show that the proposed structure provides good synchronization over a Ricean fading channel if it can be designed by the suitable estimation parameter value. The overall BER curves show that iterative carrier estimation combined with iterative decoding has negligible degradation with respect to ideal coherent detection.

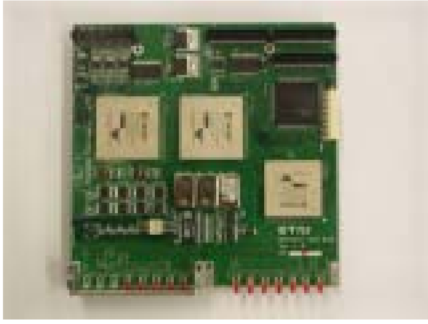

Figure 10. Demodulator Board

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