A Low-Complexity High-Throughput Soft-Output MIMO Decoder

Zhan Guo, Peter Nilsson and Viktor Öwall

Department of Electroscience, Lund University, SE-22100 Lund, Sweden

***Abstract*— A low-complexity soft-output decoding algorithm is proposed for MIMO detection. A VLSI architecture is further proposed to support high-throughput MIMO decoding. The simulation and implementation results show that the proposed algorithm and VLSI architecture can approach the performance of the conventional soft-output MIMO decoding algorithms with lower complexity and higher decoding throughput. The proposed algorithm and VLSI architecture would be promising for emerging MIMO applications such as HSDPA, 802.11n, 802.16e and 802.20. It also shows potentials for the MAGNET date rate classes.**

I. Introduction

MIMO systems are shown to be capable of achieving an extraordinary spectral efficiency near Shannon bound [1]. The optimal Maximum-likelihood (ML) decoders have been shown to be feasible for 4×4 MIMO systems with QPSK modulation [2] and [3]. However, ML decoders for the MIMO systems with higher modulation constellations are not yet available due to the complexity.

To solve and simplify the exponentially complex search problem in ML decoders for MIMO systems, lattice decoders are proposed to achieve near-ML performance with reasonable complexity [4]. An early VLSI implementation of the lattice decoding algorithm is presented in [5] for a 4×4 16-QAM MIMO system, in which a breadth-first search method is employed and coined as K-best sphere decoding (SD) algorithm. The drawback with the VLSI architecture of [5] is that the decoding throughput is limited to 10 Mb/s at a 100 MHz clock frequency. We proposed a K-best Schnorr-Euchner (KSE) algorithm in [6], which can achieve a much higher decoding throughput and lower complexity than the K-best SD.

Moreover, the lattice decoder can be extended to support soft-outputs. The most well-known soft-output lattice decoders for MIMO systems are list sphere decoder (LSD) of [7] and list sequential sphere decoder (LISS) of [8]. Both the LSD and the LISS have to maintain a large stack to calculate the soft-outputs. Hence, their complexity is larger and their decoding throughput is lower. In this paper, we propose a modified KSE (MKSE) algorithm. Compare to the LSD, the proposed algorithm can achieve higher decoding throughput with lower complexity and minor performance degradation.

II. Algorithms

Fig. 1 shows a standard flowchart of a soft-output MIMO receiver. The information bits $\mathbf{u}$ is encoded and interleaved to become the coded bits $\mathbf{c}$, which is the input to the constellation mapper. The soft-output MIMO detector takes channel observations $\mathbf{x}$, and calculates extrinsic information $L_e(\mathbf{c})$ for each of the coded bits per symbol vector. Then $L_e(\mathbf{c})$ is deinterleaved to become the *a priori* input $L_a(\mathbf{c}')$ to the outer soft-input/soft-output (SISO) decoder, which makes decisions $\hat{\mathbf{u}}$ about the information bits by *a posteriori* information $L(\mathbf{u})$.

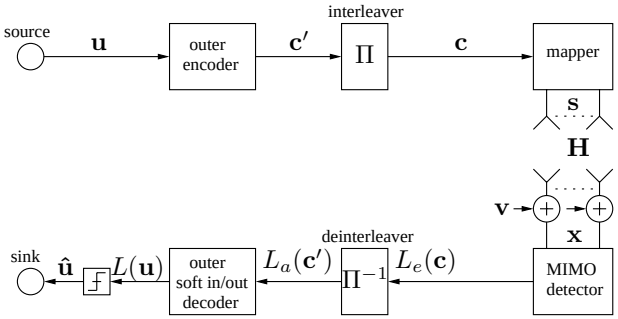


Fig. 1. MIMO transmission and receiver model

The KSE algorithm proposed in [6] is shown to outperform the K-best SD in both complexity and decoding throughput. The KSE algorithm is outlined as below:

1) At the root node, initialize one path with metric zero.
2) Extend each survivor path, retained from the previous iteration, to several contender paths, and update the accumulated metric for each path.
3) Sort the contender paths according to their accumulated metric.
4) Select the K best paths, and discard the other paths.
5) If the iteration arrives at the end node, stop the algorithm. Otherwise, go to step 2).

The best path at the last iteration is the hard output of the decoder. On the other hand, the list of paths obtained at the last iteration can be used to calculate soft outputs. The KSE thus supports soft outputs as well, though it was proposed as a hard-output MIMO decoder in [6]. Similar to the other soft-output MIMO decoders, a larger K would improve the decoding performance with the penalty in complexity. Another disadvantage with larger K is the decoding throughput, since the calculation period of the KSE is proportional to K [6].

A modification of the KSE is proposed in this paper to improve its performance without increasing K. Inspired by [8], the modified KSE (MKSE) tries to use the information

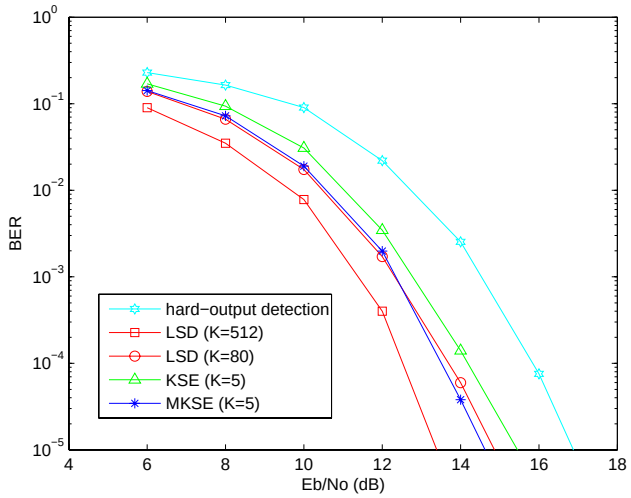


Fig. 2. Comparative simulation results, outer rate 1/2 convolutional code with memory 2, 4×4 16-QAM.

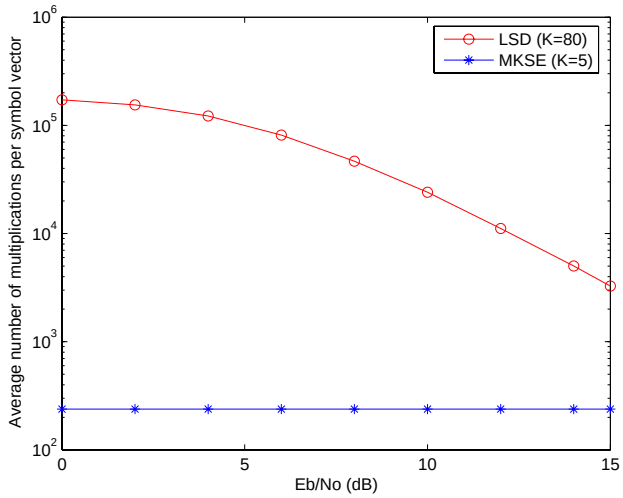


Fig. 3. Complexity comparison, 4×4 16-QAM.

contained in the discarded paths that are not fully extended to the end node [8]. In other words, The MKSE generates the soft outputs by using the discarded paths as well as the K survivor paths, with an addition to step 4) of the KSE.

- ····· From the k-th iteration, move the discarded paths to the candidate list.

The modification to the KSE is minor. Consequently, the VLSI architecture proposed in [6] for the KSE can also be applied to the MKSE with minor modifications. The MKSE has the same decoding throughput as the KSE with the same K, since both retain the equal number of survivor paths until the end node.

Both the KSE and the MKSE have advantages in hardware implementations compared to the LSD of [7] and the LISS of [8]. The KSE/MKSE is a single-direction search algorithm, i.e., the calculation proceeds in forward direction only. Consequently, the KSE/MKSE is easily implemented in a parallel and pipelined fashion achieving fixed and higher throughput. Both the LSD and the LISS are two-direction search algorithms, i.e., the calculation proceeds forward and backward. Their decoding throughput is variable, since it depends on the maximally possible search time. The variable decoding throughput may be an obstacle in a practical system.

III. Simulation Results

A 4×4 16-QAM MIMO system is considered in our simulations. To enable comparisons with the results from [7], the frame length is chosen to be 9216 information bits, and the SNR per transmitted information bit is defined as:

$$\left(\frac{E_b}{N_0}\right)_{dB} = \left(\frac{ME_s}{N_0}\right)_{dB} + 10\log_{10}\frac{1}{R_c M_c} \qquad (1)$$

where E_s is the average energy per transmitted symbol, R_c is the code rate and M_c is the number of bits per constellation symbol. To get an insight into the average behavior of a

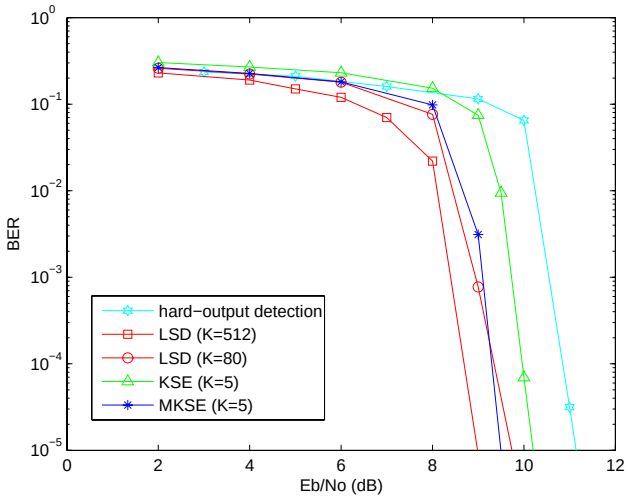


Fig. 4. Comparative simulation results, outer rate 1/2 turbo code with memory 2, 4×4 16-QAM.

MIMO receiver, all simulations herein are performed until at least 10 frame errors are incurred or at most 200 frames are transmitted. As discussed in [7], an ergodic channel model is used in the sense that the statistical nature of channel matrix is observed as the channel is used.

Fig. 2 shows comparative simulation results with an outer $R_c = 1/2$ convolutional code with memory 2. As expected, the KSE is shown to be a soft-output MIMO detector. Even the KSE (K=5) shows a limited capability in the soft values generation, taking into account that it has only K=5 paths as the candidate list.

The parameters of the MKSE simulated are K=5 and k=4, and hence the MKSE has 80 candidate paths for the soft values generation [9]. Note that the MKSE has the same performance as the LSD with a list of 80 candidates, although

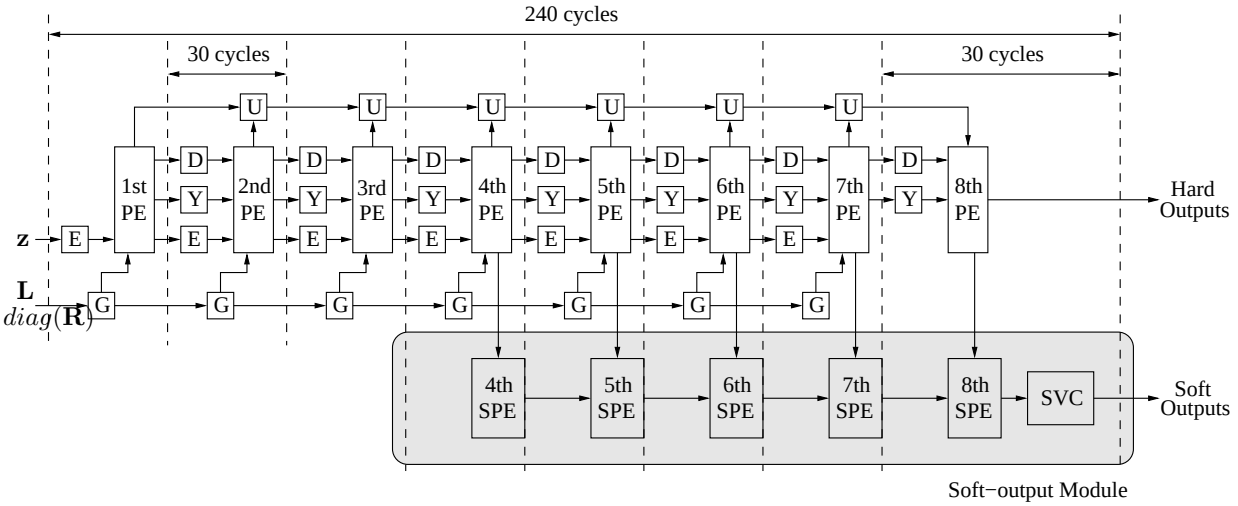


Fig. 5. VLSI architecture of the KSE/MKSE decoder for the 4×4 16-QAM MIMO system

the complexity of the MKSE (K=5) is much lower than that of the LSD (K=80), as shown in Fig. 3.

Fig. 4 shows comparative simulation results with an outer $R_c = 1/2$ turbo code with memory 2. The MKSE (K=5) outperforms the KSE (K=5) and the hard-output detection by about 0.7 dB and 1.7 dB, respectively, with only 0.5 dB loss compared to the LSD (K=512). Therefore, the proposed MKSE is also suitable for turbo coded MIMO systems.

IV. Proposed VLSI Architectures

The VLSI architecture proposed in [6] for the hard-output KSE algorithm is easily extended to support the soft-output MKSE algorithm. Fig. 5 shows the overall architecture of the decoder for the 4×4 16-QAM MIMO system. The architecture supports both hard-outputs and soft-outputs. When the soft-output module is not included, the architecture is simply a hard-output KSE decoder. Otherwise the architecture becomes a soft-output MKSE decoder.

The function of the soft-output module is to exploit the discarded paths from the hard-output module. According to the simulation results for the 4×4 16-QAM MIMO system, the MKSE should retain the discarded paths from the 4-th stage to the last stage. The MKSE does not need to keep up to 80 paths until the last stage, since the transferred data in the soft-output module is the soft values (path metrics) instead of the retained paths. The decoding period and latency of the hard-output module are not affected by the soft-output module, and hence the MKSE has the same decoding throughput as the KSE.

Compared to the hard-output KSE, the additional resources to the soft-output MKSE are 16 4-to-4 combinational decoders, 64 comparators, 64 branch-metric (BM) registers and 2 subtractors used in the soft-values-calculation (SVC) unit. However, wordlength requirements are relaxed in the MKSE compared to the KSE. The MKSE tries to find a range of better points and calculate the soft values, while the KSE tries to search the best point corresponding to the hard-output. What the MKSE focuses is not on absolute accuracy of the searched points, but on their diversity. That is also why a soft-output MIMO detector always prefers to find as many points as possible. Our fixed-point simulation results prove the statement above. As proved later in Table I, the core equivalent gates number of the MKSE is only 6.5 percent higher than that of the KSE. This penalty is worth since the MKSE supports soft-output.

V. Implementation Results

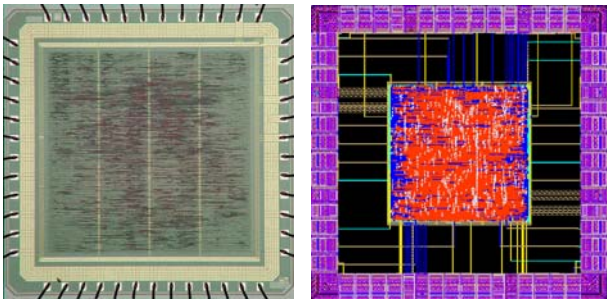
The proposed VLSI architectures are modeled in Verilog HDL, synthesized using Synopsys Design Compiler, and routed using Cadence SoC Encounter/Silicon Ensemble. The RTL and gate level netlists are all verified against the same test vectors generated from the MATLAB fixed-point model. The post-layout timing is verified using Synopsys PrimeTime with net and cell delays back annotated in SDF format [10].

A. Hard-Output KSE Decoder

The hard-output KSE decoder was fabricated in a 0.35-μm CMOS technology. Fig. 6(a) shows the die photo of the chip. The chip core area is 2.4×2.4 mm^2 with 91 K gates. For the 4×4 16-QAM MIMO system, each symbol vector contains 16 bits. The decoding throughput that the chip can support is thus equal to $\frac{16}{30} f_c$, where f_c denotes the clock frequency. The decoding latency of the chip is equal to $30 * 8/f_c$. The chip was functional at 2.8 V with a 100 MHz clock at room temperature, and could achieve a decoding throughput of 53.3 Mb/s with 626 mW power consumption.

B. Soft-Output MKSE Decoder

The soft-output MKSE decoder is to be sent for fabrication in a 0.13-μm CMOS technology. Fig. 6(b) shows the layout of the chip. The chip core area is 0.75×0.75 mm^2 with 97 K gates. The post-layout timing simulation shows that the chip can be operated at a maximal clock frequency of 200



(a) Die photo of the hard-output KSE decoder, 0.35-μm CMOS. (b) Layout of the soft-output MKSE decoder, 0.13-μm CMOS.

Fig. 6. The implemented MIMO decoders, 4×4 16-QAM.

TABLE I

SILICON COMPLEXITY COMPARISON I, 4×4 16-QAM, 100 MHZ CLOCK FREQUENCY, 0.35-μM CMOS.

	Hard-Output		Soft-Output
	K-best SD [5]	KSE	MKSE
Equivalent gates number (K)	109	91	97
Decoding throughput (Mb/s)	10	53.3	
Decoding latency (μs)	12.8	2.4	

MHz. The maximal decoding throughput of the MKSE is thus expected to be more than 100 Mb/s, and the corresponding decoding latency is 1.2 μs.

C. Silicon Complexity Comparison

Table I shows the silicon complexity comparison between the hard-output K-best SD, KSE and soft-output MKSE. The equivalent gates number is defined as the total area divided by the area of a drive-1 NAND gate. Both KSE and MKSE outperforms the K-best SD in complexity and decoding throughput.

For soft-output 4×4 16-QAM MIMO decoding, there has been one silicon implementation estimation published [11] whose complexity is estimated in a 0.18-μm CMOS process. To enable a comparison, we scaled the MKSE decoder from 0.13-μm to 0.18-μm [10]. Table II shows the silicon complexity comparison between [11] and the MKSE. The comparison results show that the MKSE can achieve higher decoding throughput with lower complexity. It should be noted that the performance of [11] is better than that of the MKSE (K=5), since [11] uses the LSD (K=256) algorithm.

VI. CONCLUSION

In this paper, the MKSE algorithm is proposed to improve the performance of the soft-output KSE with minor modifications. A VLSI architecture is further proposed for the MKSE, which is scalable to support both hard-outputs and soft-outputs. The simulation and implementation results show that the MKSE can approach the performance of the LSD proposed in [7] with lower complexity and higher decoding throughput.

TABLE II

SILICON COMPLEXITY COMPARISON II, 4×4 16-QAM, 122.88 MHZ CLOCK FREQUENCY, 0.18-μM CMOS.

	LSD (K=256) [11]	MKSE (K=5)
Area (mm^2)	8.38	1.07
Decoding throughput (Mb/s)	38.4	65.5

The proposed algorithm and VLSI architecture would be promising for emerging MIMO applications such as HSDPA, 802.11n, 802.16e and 802.20. It also shows potentials for the MAGNET date rate classes [12].

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