Low Cost Variable Delay Line for Impulse Radio UWB Architectures

Álvaro Álvarez Vázquez[1], Beatriz Quijano Ruiz[1], José Luís García García[2]

***Abstract* — This paper introduces a programmable delay line circuit suitable for Impulse Radio Ultra Wideband (IR-UWB) architectures. When dealing with Impulse Radio Technologies, fine synchronisation used to be related to relative high cost devices. The low cost, low power architecture reported, has been tested into a COTS (Commercial Off The Shelf) breadboard, but is being easily implemented into Silicon CMOS Integrated Circuits. The achieved results show good performance and delays step in the sub-nanosecond range.**

***Index Terms* — Delay line, Programmable, Variable, Impulse Radio, UWB, synchronization…**

I. Introduction

THE recent developments in wireless technologies have increased the research interest in higher data rates and low power systems for wireless ad-hoc networking. These networks allow the fast deployment of several kinds of applications, from Local Area Networks (LAN) and Personal Area Networks (PAN), to smart wireless sensor network, also covering many different scenarios, from offices and houses to open wide areas. But all these applications are mainly focused on portable and mobile systems, where power consumption is a thread, and forces the investigation of low power devices, while keeping an average cost required for market success.

In this field, Ultra Wideband is a promising radio technology for wireless ad-hoc networking. UWB is defined as any communication system where the fractional bandwidth is greater than 0.25 or occupies 500 MHz or more of the radiated spectrum.

There are several UWB modulations alternatives, from Multi Band Orthogonal Frequency Demultiplexing (MB-OFDM) to Direct Sequence Code Division Multiple Access (DS-CDMA), but the original one and most attractive in terms of combining communications with positioning or location capabilities is the Impulse Radio UWB. This technique is based on the broadcasting of very low power radio signals by the transmission of very short, in the sub-nanosecond range, electrical pulses, which are translated into large bandwidths in the frequency range. In IR-UWB transmitter and receiver must be coordinated to send and receive pulses with enough accuracy to correctly demodulate the data bits, coordination that must be done both at PHY and MAC layers. MAC coordination corresponds to time slots assigned for each user, but also MAC depends on correct PHY "coordination", which is done through accurate clock synchronization.

This paper describes a low cost, low power, simple circuit suitable for fine clock synchronization in IR or UWB CDMA receivers, providing variable time delays in the nanosecond and sub-nanosecond ranges

II. Motivation and Applications

The purpose of this architecture is to allow fine synchronization in the sub-nanosecond range for UWB Impulse Radio receivers. The synchronization is a key parameter in the reception of IR signals, since it is required for signal correlation, energy capture, delay estimation, location and positioning applications and data demodulation. The architecture has been developed and tested with signals up to 80 MHz, in order to test the fundamentals and operational basis, although it could be upgraded to higher frequencies following the same structure.

This circuit has been tested with On-Off Keying, (OOK) Dis-Joint Pulse Position Modulation (DJ-PPM), and simple Direct Sequence-Spread Spectrum (DS-SS) signals, integrating the delay line in the receiver front-end, between the master clock and the sampling unit and analog-to-digital converter. In an OOK IR system, the data is modulated following a too simple approach, a pulse is sent when there is a logical '1' and no pulse when there is a logical '0'. Following this modulation approach, frequency requirements of the delay circuits are relaxed, since they are applied just to the master clock which determines the presence or absence of UWB pulses. This master clock is directly related to the Pulse Repetition Frequency (PRF), and therefore, related to the system throughput and data rate. Master clocks in the order of 20 MHz, are theoretically able to achieve 20 Mbps just with OOK, while combined with Pulse Amplitude Modulations can reach several tens of Mbps.

The authors would like to thank the European Commission for the financial support of part of this work in the IST European Research projects U.C.A.N. (IST-2001-32710) and FP6 Integrated Project PULSERS (FP6-506897)

Alvaro Alvarez Vazquez and Beatriz Quijano Ruiz are with Advanced Communications Research and Development S.A. (ACORDE), U. Of Cantabria, Avda. Los Castros s/n, 39005 Santander, SPAIN (phone: +34 942 200923; fax: +34 942 290404; e-mail: alvaro.alvarez@acorde.biz, beatriz.quijano@acorde.biz).

Jose Luis Garcia is with the Communications Engineering Department, U. Of Cantabria, Avda. Los Castros s/n, 39005 Santander, SPAIN (phone: +34 942 201491; fax: +34 942 290404; e-mail: jlgarcia@dicom.unican.es).

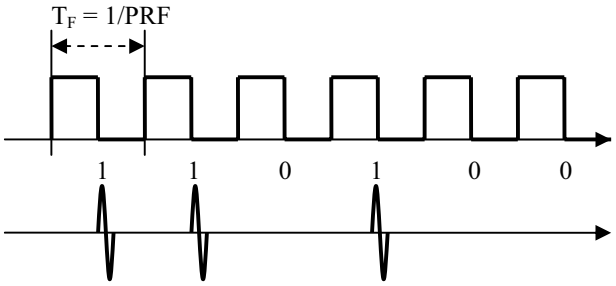

Figure 1: OOK IR-UWB master clock vs. signal

In the OOK, DS, DJ-PPM cases, where the pulse distances are fixed, and can be controlled with a "low" frequency clock (i.e. 20 MHz), the main synchronization problem comes from the fact that the Tx and Rx master clocks may be fixed in frequency (topics related to stability may be solved with re-synchronization techniques thought fine adjustments), but with a phase misalignment

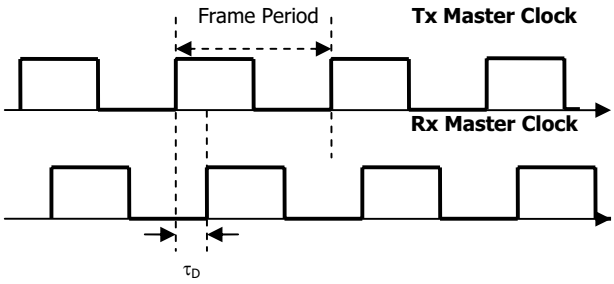

Figure 2: Delay or phase misalignment between clocks

The Receiver master clock might have an initial delay τ_D (dependent on the intrinsic phase difference of both Tx and Rx clocks, plus the propagation delays), which could be compensated at the signal acquisition module thought the variable delay line.

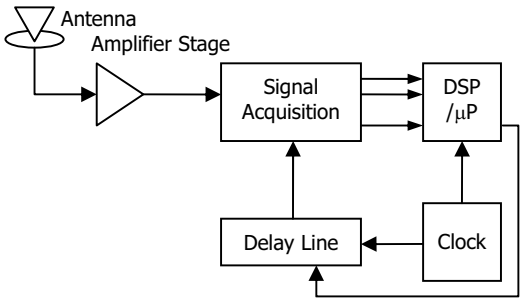

Figure 3: Receiver architecture basis

With the programmable delay line, we must be able to synchronize the incoming pulses with the Signal Acquisition module, and therefore, process and demodulate the incoming signals. Moreover, simple hardware added to this proposed architecture, designed to reduce the receiver/transmitter latency, can be integrated in order to facilitate the location properties of the IR-UWB system.

III. Approach

For digital circuit applications, clock distribution, and path compensations, there are some commercial available delay line products, but they are fairly expensive for the UWB applications and hybrid system designs. Some of these alternatives are based on a matrix of fixed delays or cumulative fixed delays, implemented by transmission lines or inductances. This solution makes the circuit large in size, and requires fine manufacturing processes in order to achieve enough accuracy in the additive delay line structure.

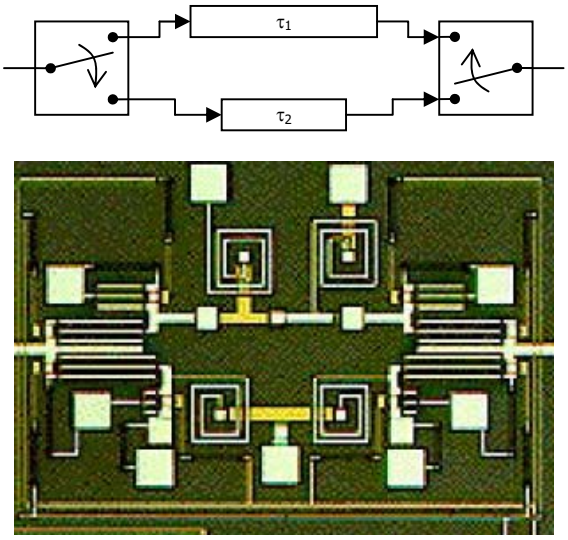

Figure 4: Delay or phase misalignment between clocks

Other approaches make use of logic circuitry, like counters or a chain of inverters or logical gates, to get at the output the input signal, delayed a variable amount of nanoseconds. However, both approaches make use of variable-length delay lines with internal connections to generate the final delay at the output. Unfortunately, most of the commercial available delay lines are not able to delay the signal in excess of the pulse period, working just up to the 30%-40% of the input pulse width, and only few ones allow delay times greater than the pulse width.

I.e. Maxim/Dallas Semiconductor has programmable delay lines that reproduces an input logic state at the output after a user-programmed delay, but only a family set provides also integrated on-chip reference delay and the capability of delaying clock signals up to and beyond a full cycle, allowing complete control capabilities on the synchronization for the UWB sampling and energy capture module.

IV. Circuit Description

The architecture reported in this paper allows delays larger than a pulse period, facilitating the synchronization through a delay swept with a programmable interface, as it is shown in figure 3. It provides programmable timing capabilities and on-board resources for extending its range of applications. As a delay line it can be used for fine-tune timing systems, work as

a pulse width modulator or just as a phase controllable oscillator (suitable for advanced MIMO architectures).

A. Delay Circuit Basis

The basic idea is to propagate the reference clock signal through the circuit and include a variable delay in the propagation of the reference sampling clock. The simplest delay circuit can be implemented with a RC network, where a resistor and a capacitor are connected at the output of the input buffer. When the logic state changes from '0' to '1', the capacitor begins to charge, and therefore the voltage at the output starts rising to the high level following an exponential approach:

$$V_C = V_{'1'} \cdot e^{-\frac{t}{\tau}} \qquad V_{DC} = V_{'1'}\left(1 - e^{-\frac{t}{\tau}}\right)$$

Both charge and discharge processes are characterised by an exponential law, however, from our particular point of view, we have paid attention just to the charge process in order to characterise the rising edges at the input gate of an output buffer stage. The RC network works as a low pass filter, therefore, it smoothes the fast transition at the input from 0 to V Volts, and with a comparator circuit or a buffer amplifier based on a threshold voltage, is it possible to recover the square input signal, just with the delay introduced by the charge time of the capacitor.

At the output of the RC network, we have placed a comparator circuit working as signal buffer, because the voltage on the capacitor terminals follows an exponential equation, and we needed a square type signal, "cleaning" the delayed signal.

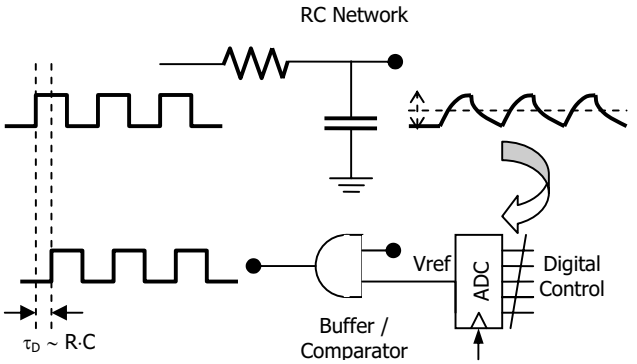

Figure 5: Delay RC circuit

As a result, the delay placed into the incoming signal depends on three parameters:

1) $\tau = R \cdot C$
2) The threshold voltage reference (Vref)
3) The comparator gate propagation delay

One is fixed (propagation delay), and two are variable, therefore, in this architecture, variable delays can be easily achieved varying the value of the RC network, i.e. replacing the resistor by a potentiometer, or adjusting the Vref value with a Digital to Analog Converter (DAC).

Both alternatives can be digitally controlled (digital potentiometer, or DAC), with a data bus, serial or parallel. In the design tested in this work, a traditional screw rotation potentiometer was implemented in order to check the reliability of the circuit, but an improved version is being designed with fully digital programmable control.

However, this delay circuit has an important drawback, related to a full cycle delay. Since it is based on the delay introduced by the charge and discharge process of a capacitor, it is not possible to introduce a delay exceeding the 40-50 % of the incoming pulse or clock cycle. Therefore additional circuitry is required to perform the full cycle delay.

B. Circuit Schematic

Based on the RC network delay with an output signal conditioner (buffer or comparator), suitable for delays up to 40 % of the pulse width, we can not delay our input signal up to a full cycle, but we are able to delay a signal derived from the input, but with larger pulse width, i.e. making use of a divider, and then combine both signals in order to reconstruct a signal tuned at the original input frequency, but delayed in time, as is represented in figure 6. Since the signal from the divider has lower frequency (f_O/N), consequently it has larger periods, and therefore it is possible to delay this signal up to the 40% of its pulse width, implying a delay in excess of a full cycle when compared to the original input.

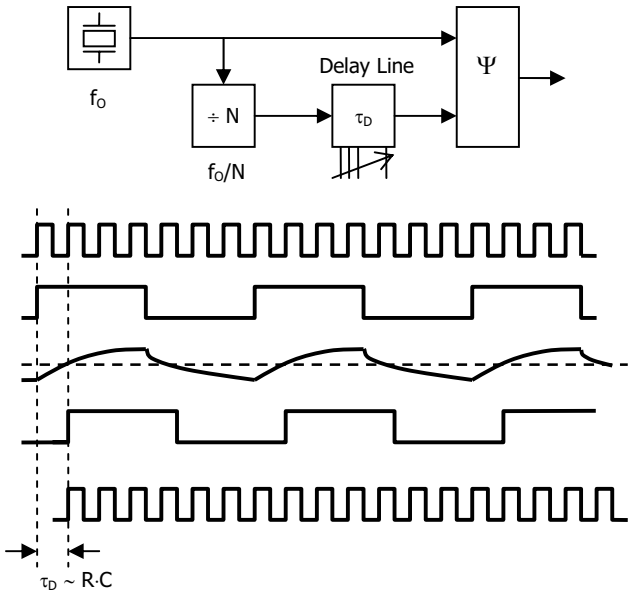

Figure 6: Full cycle delay

In order to reconstruct the signal, it was required to have a circuit able to follow the rising edges of the delayed signal as well as to be tuned at the original signal frequency (f_O) instead of the delayed signal (f_O/N). This could be done with a VCO running at the original frequency, and a Phase Locked Loop, able to compare the phases (equivalent to delay in the pulse edges) of the signals coming from the delay line and the VCO. To be able to compare both signals, it was needed to add an additional clock divider at the output of the VCO.

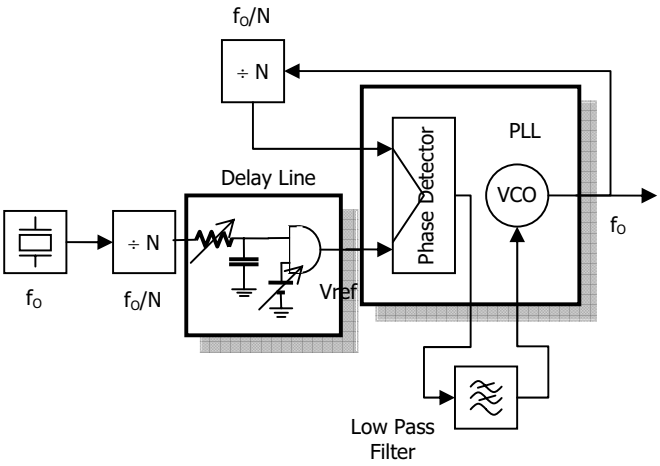

Figure 7: Full cycle delay

Figure 7 shows the schematic of the whole delay line circuit. The core of the delay block consists of a RC delay network, and a buffer or comparator which rebuilds the delayed clock signal, as well as allows variable delay according to the voltage threshold on the logic gate.

The rest of the circuit is based on a PLL structure and a set of frequency dividers in order to increase the pulse width and facilitate the full cycle delay. Additionally a low pass filter is placed between the phase detector and the VCO, as in described in the PLL architectures.

C. Designed Circuit

In order to perform fast validation of the architecture and test the circuit behaviour, an integration breadboard was designed with commercial components placed into a PCB. Further designs are currently under developing stages in order to implement the full system in a small (below 1 mm^2) and low power CMOS Integrated Circuit.

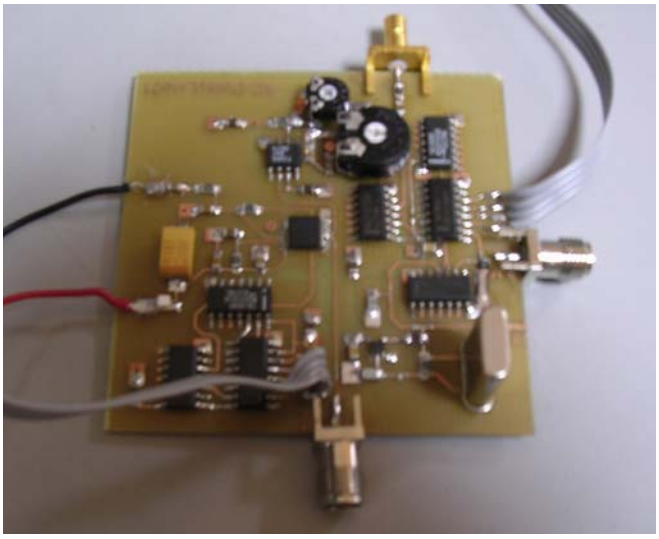

Figure 8: Developed Test Breadboard

Figure 8 shows a picture of the tested breadboard. The original clock has been implemented with a forward biased inverter oscillator, tuned at 10 MHz with a low cost crystal. This clock feeds a frequency divider made of CMOS counters and flip flop gates, and then driven to the RC network connected to a comparator gate, based on a broadband Operational Amplifier. The output of the comparator stage is fed into the phase detector of the PLL chip (Texas Instruments TLC low cost/low power VCO + Phase/Frequency Detector), where is compared to the divided signal coming from the VCO output.

Since the signal for the crystal oscillator is centered at 10 MHz, the output of the VCO is also tuned at 10 MHz. The only difference between both signals is a phase misalignment (time delay) due to propagation delays of the logical gates (fix delay) plus the variable delay from the RC and comparator networks.

V. Test and Results

The circuit has been measured and characterised making use of a 500 MHz High Speed Digital oscilloscope, allowing resolutions on the sub-nanosecond range. The results have shown a perfect behavior of the delay line, with variable capabilities, through the control of both potentiometer of the RC network or the DAC, used as voltage reference for the comparator gate.

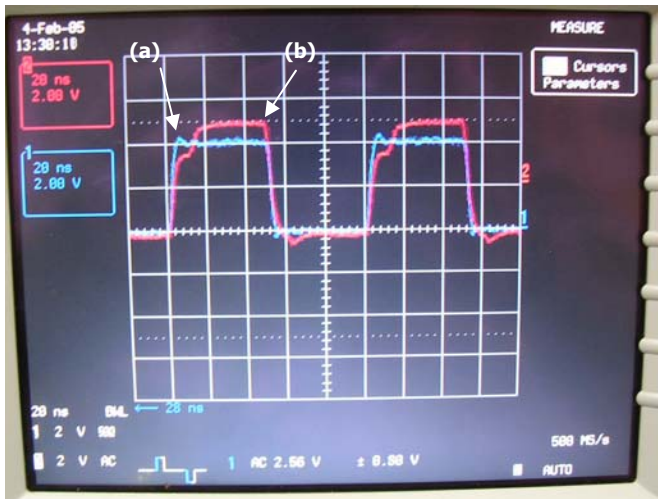

Figure 9: Input and Ouput signals without delay

Figure 9 shows the input (a) and output (b) signals from the delay line circuit. In this case the values of the potentiometer and/or DAC has been adjusted in order to compensate the delays introduced by the internal digital gates, and show a synchronous signal at the input and output ports. Please note that the output signal has not been cleaned with a buffer stage, so small peaks appear on the picture. In the next version, an output buffer for signal conditioning is being designed.

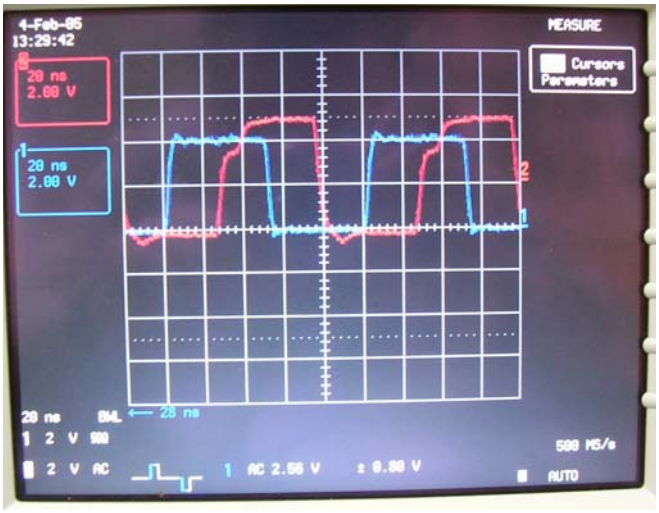

Figure 10: Input and Ouput signals with 25 ns delay

Figure 9 shows the same signals when the potentiometer has been adjusted to 25 ns of delay. With this circuit we were able to achieve delays in excess of the whole clock cycle, i.e. delays larger than 100 ns in 500 ps steps.

VI. Conclusion

A digitally programmable delay-line concept and architecture have been designed, developed and tested in order to provide simple, low cost, low power circuits for the implementation of phase/delay clock adjustment, as well as synchronization modules for many different applications, such as Impulse Radio OOK or DS-CDMA transmitters and receivers. The design makes use of simple circuits combined all together in order to achieve good performance, fine timing precision and fast circuit implementation. The core of the architecture is based on a RC delay network and a PLL module composed of a VCO and a phase/frequency detector.

This circuit has been tested in laboratory showing delay lines in excess of the input pulse width and time steps below the nanosecond range. Moreover, this architecture is currently under CMOS Silicon Integrated Circuit implementation, in order to obtain a chipset to be placed in a Ultra Wideband receiver demonstrator.

References

[1] M. Z. Win and R. A. Scholtz, "Impulse radio: How It Works" IEEE Communications Letters, Vol. 2, Issue 2, pp. 36-38, February 1998

[2] E.C. Kisenwether, "Ultrawideband (UWB) Impulse Signal Detection and Processing Issues," IEEE Tactical Communications Conference 1992, Vol. 1, pp. 87-93, 1992

[3] M.G.M. Hussain, "Ultra-Wideband Impulse Radar-an Overview of the Principles," IEEE Aerospace and Electronics Systems Magazine, Vol. 13, Issue: 9, pp. 9-14, September 1998

[4] R.A. Bechade and R.M. Houle "Digital delay line clock shapers and multipliers", IBM J. Research and Development, Vol. 39 Nº ½ January/March 1995.

[5] Fernando Noriega, Pedro Gonzalez, "Designing LC Wilkinson Power Sppliters" Aug 1, 2002, RF Design (RF and Microwave Technology for Design Engineers)

[6] A. Efendovich, Y. Afek, C. Sella and Z. Biwosky, " Multifrequency Zero-Jitter Delay Locked Loop" IEEE J. Solid State Circuits 29, Nº 1, pp. 67-70, January 1994

[7] Maxim Semiconductor, "How Delay Lines Work", App Note 209, http://www.maxim-ic.com/appnotes.cfm/appnote_number/1178 , APP 1178, Aug 30, 2002

[8] Maxim Semiconductor, "Using Programmable Delay Lines", Tech Brief 38, http://www.maxim-ic.com/appnotes.cfm/appnote_number/992 , APP 992: Mar 05, 2002

[9] M. Johnson and E. Hudson, " A variable Delay Line PLL for CPU-coprocessor synchronization" IEEE J. Solid-State Circuits 23, Nº 5, 1218-1223, October 1988

[10] N. Orlanovic, R. Raghuram and N. Matsui, "Characterization of microstrip meanders in PCB interconnects," Electronic Components and Technology Conference, Conference Proc., May 21-24, 2000.

[11] O. M. Ramahi, "FDTD analysis of conventional and novel delay lines," Presented at the 16th Annual Review of Progress in Applied Computational Electromagnetics meeting, Monterey, CA, March 20-25, 2000.

[12] W. Lindsey and C.M. Chie, " Asurvey of Digital Phase Locked Loops", Proc. IEEE 69, 410-431, April 1981

[13] Maxim Semiconductor, "Delay Lines Comparison", App Note 229, http://www.maxim-ic.com/appnotes.cfm/appnote_number/1812 APP 1812: Dec 10, 2002

[14] Zeljko Zilic, "Phase- and Delay-Locked Loop Clock Control in Digital Systems" McGill University, Montreal, www.techonline.com

[15] W. J. Gleeson and J. R. Young, "Digital Self-calibrating Delay Line and Frequency Multiplier" International Patent WO 93/13598, July 8, 1993

[16] James R. Burnham, Gerard K. Yeh, Enoch Sun, Chih-Kong Ken Yang, "Design and Analysis of a Jitter-Tolerant Digital Delay-Locked-Loop Based Fraction-Of-Clock Delay Line" IEEE International Solid-State Circuits Conference – Session 19 – Clock Generation and Distribution, ISSCC 2004.

[17] Joonbae Park, Yido Koo, Wonchan Kim, "A Semi-Digital Delay Locked Loop for Clock Skew Minimization", 12th International Conference on VLSI Design - 'VLSI for the Information Appliance' p.584, January 10 - 13, 1999 Goa, India