On the Architectural Design of Frequency-Agile Multi-Standard Wireless Receivers

Linus Maurer, DICE, Linz, Austria,
Thomas Burger, ETH Zürich, Switzerland,
Thomas Dellsperger, ACP Zollikon, Switzerland,
Rainer Stuhlberger, Gernot Hueber, University of Linz, Austria,
Matthias Schmidt and Robert Weigel, University of Erlangen, Nuremberg, Germany

email: linus.maurer@infineon.com

ABSTRACT

A flexible, reconfigurable receiver architecture that extends the direct conversion architecture is presented. The receiver structure is based on high dynamic range/low-power ΣΔ analog-to-digital converters (ADC) and digital signal processing functions implemented locally on the radio frequency integrated circuit (RFIC). This relaxes requirements for the analog part of the receiver and enables configurable receive-bandwidths, because channel filtering is realized in the digital domain. Since analog building blocks have limited reconfiguration capabilities by nature of their implementation, the extension of the conventional analog signal processing blocks by a digital front-end (DFE) greatly enhances the flexibility of the RFIC. Key building blocks for the proposed receiver, such as tunable RF filters, ADC and DFE building blocks are discussed.

I. INTRODUCTION

The software defined radio (SDR) idea was started in the early '90s by J. Mitola when he published his vision of an idealized software radio [1]. Direct sampling of the RF signal from the antenna by an analog to digital converter (ADC) should allow maximum flexibility, since all the signal processing operations could be carried out in software on a digital signal processor (DSP).
The ideal SDR architecture provides some gain at RF followed by an anti-aliasing filter directly in front of the ADC. As a consequence the ideal SDR requires block specifications for the analog/mixed signal (AMS) blocks that are technically not feasible in the short and medium term. Therefore, it has mainly remained a subject of academic study so far.
Figure 1 introduces a step forward of current RF receivers, which are mainly optimized for a single wireless standard. This architecture consists of an analog hardware section from the antenna down to the ADC, which is flexible enough to accommodate the different RF requirements of the corresponding standards.
Since analog blocks are less amenable to reconfiguration, it is advisable to shift analog signal processing tasks such as channel selection filtering to the digital domain to obtain more flexibility. As a consequence the requirements on the ADC increase, but are still relaxed as compared to the original SDR, because the ADC has to cope with a base-band rather than an RF signal. The realization of the architecture in Figure 1 will combine the analog and digital front-end (DFE) part in a single radio frequency integrated circuit (RFIC). This change is a key enabler for a fully digital base-band MODEM-IC that does not require an analog macro, since all AMS blocks are shifted to the RFIC. Thus, the MODEM-IC can be easily shrunk to future CMOS technology nodes saving development costs and shorting design cycles.

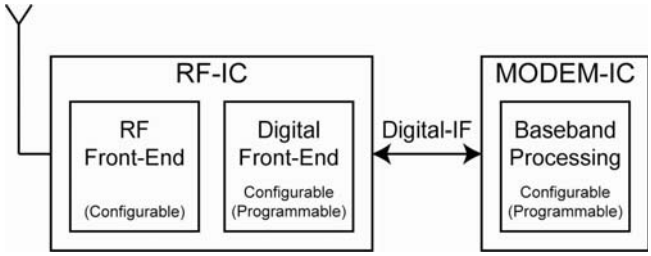

Fig. 1: Flexible RF receiver architecture.

State-of-the-art RF transceivers rarely employ digital signal processing capabilities on the RFIC. Digital functions mainly focus on control interfaces (e.g. PLL programming) and calibration functionality (e.g. analog filter tuning). The pre-dominant interface between the current RF and base-band ICs is still the analog IQ-interface. With the DFE concept, this analog data interface will be replaced by a digital one. The step requires signal decimation and filtering in the DFE, to reduce the excessive data rates at the ADC outputs.
With the advent of RF-CMOS the above approach has become technically feasible and also economically reasonable. Utilizing digital signal processing functions will boost the re-configurability of the RFIC and results in a future proof architecture, since RF-CMOS is gradually becoming the main semiconductor technology for RFICs targeting wireless applications.

II. STATE-OF-ART RECEIVERS

The direct conversion receiver (DCR) of Figure 2 has replaced the heterodyne receiver as predominant architecture for wireless applications. It has a lower

number of building blocks at RF than its heterodyne counterpart. The intermediate frequency (IF) filter needed by the heterodyne architecture is replaced with low-pass filters that can easily be integrated. Further advantages of the DCR are:

- No image frequency problem at down-conversion.
- Base band processing can be implemented in a main stream technology such as CMOS.
- Programmable base band filter and ADC with digital post-filtering can all be realized in the same technology.

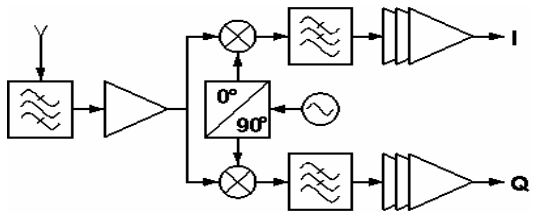

Figure 2: Direct conversion receiver architecture.

The main disadvantages are:

- LO self-mixing: the local oscillator has limited isolation to the RF path. A part of the LO signal leaks into the RF path, is down-converted to base-band by the mixer and results in an unwanted DC-offset.
- Large amplitude modulated signals are converted to the base band section via second order distortion of the IQ-mixers leading to time varying DC offset. In order to prevent this kind of DC-offset, a large second order intercept point (IP2) of the IQ-mixers is necessary (see Figure 3).

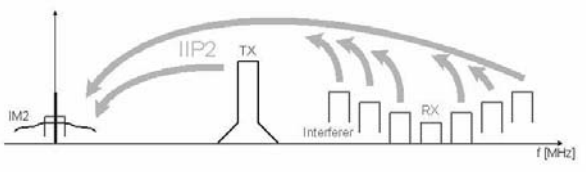

Figure 3: DC offset generation via mixer IP2.

- The signal processing at base-band is subject to considerable flicker noise from the preceding mixer stage in CMOS implementations.
- Because no intermediate stage amplification and filtering takes place the requirements for the base band filter linearity and noise are more demanding as for the heterodyne receiver.
- I/Q amplitude and phase mismatches can be a critical issue for the DCR-topology [2].

III. PROPOSED FREQUENCY AGILE RF-RECEIVER ARCHITECTURE

Figure 4 shows a block level diagram based on the DCR partitioning of Figure 2. The low-pass filters in Figure 4 only realize anti-aliasing and dynamic range reduction functionalities for the ADCs. They are not used as channel selection filters like in the conventional DCR architecture. To relax the filter specifications, an over-sampled ADC architecture is proposed. ΣΔ-ADCs are well suited because they consume low power and simultaneously provide high dynamic range. To reduce the sampling rate of the ADC cascaded-integrator-comb (CIC) filters are used. The wave-digital-filter (WDF) structure is added for channel selection together with a Finite-Impulse-Response (FIR) filter, which is also utilized for amplitude ripple equalization and pulse filtering. CIC and WDF filters are chosen due to their efficient implementation in terms of die area and power consumption. It should be noted that the CIC and WDF filters can only alter the sampling frequency by integer factors. Thus, the rate after the FIR filter is always connected to the ADC sampling rate by an integer factor. To realize fractional changes of the sampling rate, a fractional-sample-rate converter (FSRC) is added. A configurable all-pass (AP) block corrects the group delay ripple, which is mainly caused by the WDF filters.

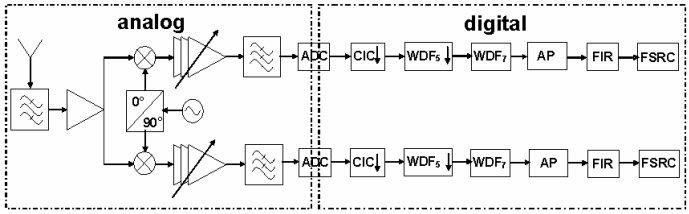

Figure 4: Proposed DFE enabled frequency agile DCR architecture.

IV. KEY BUILDING BLOCKS OF FREQUENCY AGILE RF-RECEIVERS

A. Tunable Band-Pass Filters

Figures 5 and 6 show a subset of frequency bands that a tunable band-pass filter in a cellular multi-standard receiver should cover. In order to relax requirements it is advisable to split the frequency range into two parts, one band from 810 MHz to 960 MHz and another from 1477 MHz to 2170 MHz. The sub-ranges correspond to a tuning range Δf/f of approximately 15% and 30%, respectively.

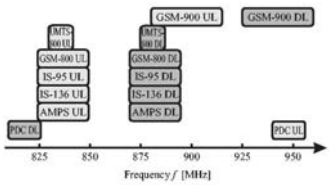

Figure 5: Worldwide spectrum allocation 0.8 – 1 GHz.

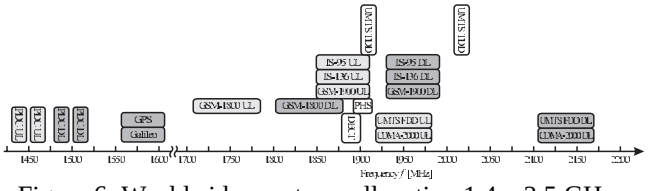

Figure 6: Worldwide spectrum allocation 1.4 – 2.5 GHz.

In the last years different attempts have been made to realize tunable filters utilizing a wide range of different technologies:
At first glance a tunable FBAR (Film Bulk Acoustic Resonator) or SAW (Surface Acoustic Wave) filter would be desirable in terms of size and amenability to integration. In [3], a thermally tunable FBAR band-pass filter with a very low insertion loss of 2.6 dB and a small size of 2x2mm^2 is introduced. With a frequency shift of only 17 MHz it does not fulfill the requirements. Another severe problem is the high power consumption of 510 mW for the heating line. A magnetically tunable SAW resonator investigated in [4] suffers from the same problems. With a demonstrated tuning range of 1.2% it can only be considered as a first step.
A more promising approach using conventional semiconductor varactors was made in [5]. Using LTCC (Low Temperature Cofired Ceramics) technology a compact duplexer module (5.7x5.7 mm^2) with a maximum insertion loss of 3.5 dB was realized. With a tuning range of 10% at a tuning voltage of 4 V it was possible to switch between the GSM1800 and GSM1900 bands.

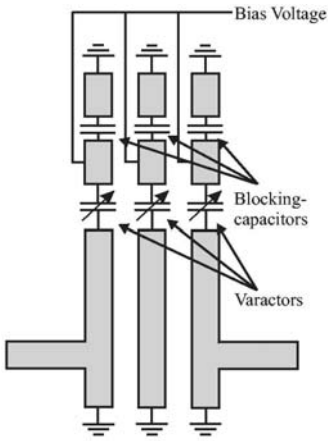

Figure 7: Structure of a tunable combline filter.

A higher tunability was reported in [6] with nonlinear dielectric varactors also embedded in a LTCC module. Achieving a tuning range of 16% the presented results are promising but the insertion loss of 4.3 dB is not acceptable for many wireless applications. To reduce size and to achieve the desired filter characteristic a three-pole asymmetric combline filter structure (Figure 7) integrated into multiple LTCC layers was used. Capacitors tunable from 2 pF down to 1.4 pF were mounted on the top of a module with a size of 7.5x6.5x2.0 mm^3.
A technology that is capable to realize the required tuning range today is distributed Micro Electro Mechanical Systems (MEMS) transmission line filters. In [7], such a filter with a tuning range of 35% is shown. The main drawback of this concept is the required switching voltage of 40 V for the bi-stable MEMS switches to load the micro-strip resonator sections and tune the inter-resonator coupling. Due to the discrete switching states it is not possible to tune the filter continuously. Further, the waveguide structure allows small filters only to be realized at high frequencies. The filter of [7] has a size of 8.9x4.2 mm^2 at a center frequency of about 8 GHz. This technology makes small filters for cellular applications hard to realize.

B. ADC
Building block requirements for a wireless receiver are closely linked to the choice of the overall receiver architecture. On the other side, they also reflect the state-of-the-art for the implementation of a particular functionality. In this sense the proposed receiver architecture is a direct consequence of progress in high dynamic range, high linearity ADCs in the past years.

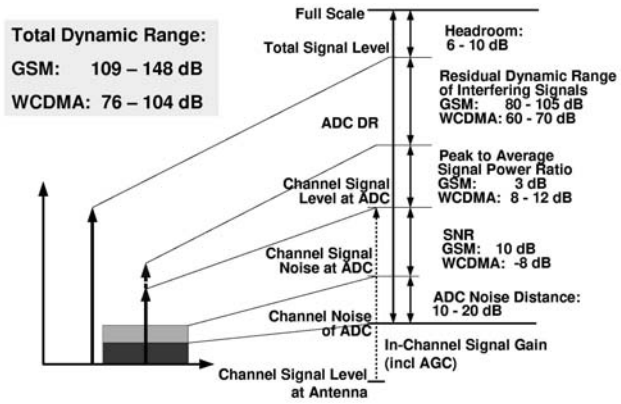

Figure 8: Dynamic range considerations for a GSM/WCDMA broadband converter.

Generally, the dynamic range of a radio signal at the antenna of a wireless base station or terminal is in the order of 80-100 dB for short distance systems such as e.g. WLAN and more than 100 dB for longer distance links as found in cellular applications. Such dynamic range is tolerable at RF where signal processing can be done at low impedance (thus not violating the low voltage headroom of advanced process technologies) with acceptable power consumption. Figure 8 shows a calculation of the required ADC dynamic range for cellular applications in a DCR with no or only a small amount of filtering (expressed as residual dynamic range of interfering signal). Keeping such high dynamic range for the ADC would lead to excessive power consumption. This is not desirable and also not necessary because the detection of the wanted radio signal can be achieved with 40-60 dB of dynamic range, including margins for the signal fluctuation. The recent development in design of ADCs for wireless terminals has led to implementations with 70-90 dB of dynamic range at acceptable power levels [8-11]. The additional dynamic range above the one needed for signal detection can now be used to simplify the design of the analog front-end. Especially the selectivity of the analog BB-filter can be relaxed, i.e. different radio standard can use the same or only a slightly modified analog BB-filter while channelization is done in the digital domain.

For the realization low power converters with a dynamic range in the order of 70-100 dB based on ΣΔ modulation are currently preferred. ΣΔ converters offer an inherent trade-off between bandwidth and resolution due to their ability to spectrally shape the quantization noise. The high gain, tracking loop architecture with a small number of DAC levels leads to high linearity with moderate gain and matching requirements for amplifiers and passive components, respectively. This is in contrast to pipe-lined converters where linearity directly depends on the matching of devices. Also, the hardware complexity of ΣΔ–converters is lower than that of their pipe-lined counterpart, especially when combining the necessary decimation with the other functionalities of the DFE.
The use of over-sampling for the ADC lowers the input referred thermal noise power with respect to signal power by the factor of the over sampling ratio. This fits modern deep sub-micron CMOS technologies well, where plenty of speed is offered from transistor devices but voltage headroom is limited.

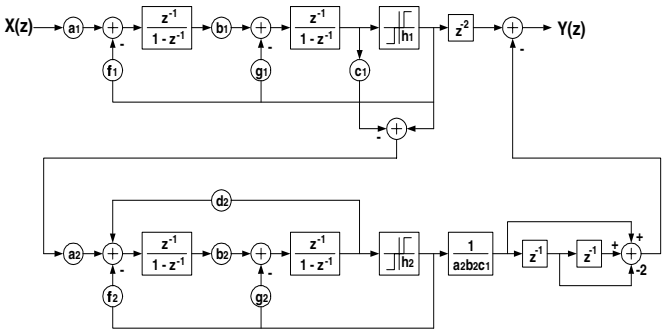

Figure 9: Multi-standard ΣΔ modulator topology.

A possible realization of the ADC is shown in Figure 9. This delta-sigma-modulator has been designed for the combination of GSM/UMTS and WLAN standards. It achieves a signal-to-quantization noise ratio (SNQR) of more than 100 dB for GSM, 89 dB for W-CDMA and 71 dB for WLAN, at over-sampling ratios of 96, 16 and 10, respectively. The modulator consists of a 4th order 2-2 cascaded topology with two 3 level quantizers to improve the SNQR at low over-sampling ratio while keeping the out-of-band noise at an acceptable level.

C. DFE

Channel selection filtering and decimation are the main tasks of the DFE introduced in Section III. The proposed DFE implementation realizes these functions by providing highly configurable filter blocks, which are adapted to the respective standard requirements. Thus, implementation effort is minimized. To further increase the flexibility of the DFE the sequencing of the different blocks with the exception of the CIC filter can be changed.
A CIC filter is used to decimate the ADC output signal by an integer factor [12]. The Nth-order CIC decimator is built of N cascaded integrators clocked at the ADC's output rate, followed by a configurable sample rate reduction and N cascaded comb stages running at the reduced output rate.

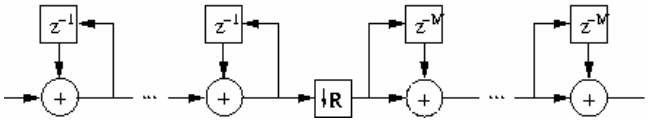

Fig. 10: Block diagram of a N-th order CIC decimator.

The transfer function of the CIC with a rate reduction R is given by $H_{CIC} = (1-z^{-RM})^N/(1-z^{-1})$. The delay mode M defines the number of delay elements used in the comb stage. Due to the filter's simplicity – integrator and comb stages are only built of adders – integer sample rate conversion is performed at minimum effort in terms of IC area and power consumption.

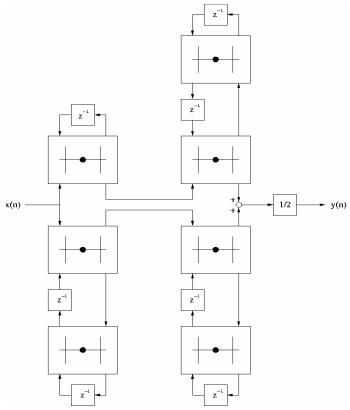

Figure 11: Block diagram of the 7th order lattice lowpass WDF.

Channel selection filtering and the final integer decimation is realized by WDFs [13]. A 5-th order WDF with fixed coefficients in half-band configuration is used for decimation by 2 and a 7-th order WDF depicted in Figure 11 with fully configurable coefficients performs most of the channel selection.
The Nth-order lattice low-pass WDF is built of N adaptors. Each adaptor requires one hardware multiplier. Since the adaptors are all-pass stages, only the signal phase changes.
A FIR filter is used for two reasons. First, pulse shapes vary among the different wireless standards under consideration, so the FIR implementation must have fully configurable filter coefficients. Second, the FIR filter acts as equalizer to reduce the amplitude ripple in the pass-band introduced by CIC and WDF stages. To correct the pass-band group delay ripple a configurable AP is used.
The ADC of the proposed architecture is normally driven by a fixed sampling clock. If the digital interface towards the base-band should deliver samples at an integer multiple of the desired standard`s symbol rate, a fractional sample rate conversion must be implemented. Normally, the rate of the digital interface should be as low as possible. The Nyquist theorem dictates that the lowest possible data rate at the digital interface is two times the respective

symbol/chip rate. In some cases it is advantageous for the succeeding digital base-band processing to realize higher interface data rate, e.g. four times the symbol/chip rate.

C. Simulation Results

A simulation chain of the proposed DFE architecture together with a ΣΔ-ADC model has been implemented. The ADC model had a dynamic range of 93 dB in a 2 MHz bandwidth and a sampling rate of 104 MHz. The signal fidelity obtained after the DFE was checked by means of Error-Vector-Magnitude (EVM) simulations. These simulations were performed with and without adjacent channels.

The left side of Figure 12 shows the signal at the ADC input for the UMTS adjacent channel selectivity (ACS) testcase. The power level of the adjacent channel is 40 dB larger than the power of the desired frequency channel. The right side of Figure 12 clearly shows that the adjacent channel is suppressed by at least 80 dB at the DFE output. Simultaneously, the signal is decimated to four times the UMTS chip-rate of 15.36 Mcps. The resulting EVM at the DFE output is 1.8% without adjacent channel and 4% with adjacent channel.

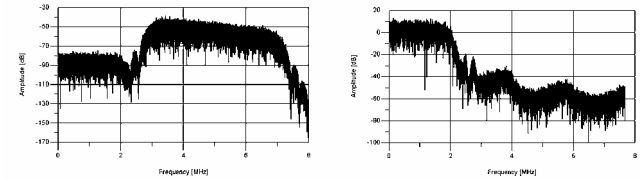

Fig. 12: ADC input and DFE output spectrum for the UMTS ACS-testcase

The left side of Figure 13 shows the signal at the ADC input for the IS95 single tone desensitization test case. The interferer signal has a frequency modulation with a bandwidth of 30 kHz and a frequency offset of only 900 kHz from the center frequency of the desired signal. The power of the interferer signal is 71dB above the desired signal level. After re-configuration of the DFE to the IS95 channel bandwidth an EVM simulation yields 3.3% without interferer and 7% with above described interferer at four times the IS95 chip-rate of 4.9152 Mcps. The adjacent channel suppression of the DFE is 121 dB.

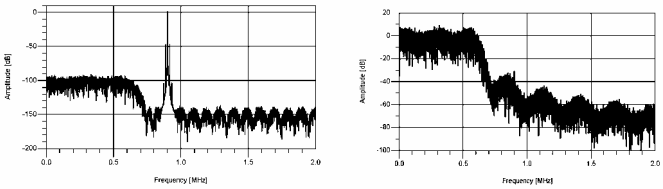

Fig. 13: DFE input and output spectrum in IS-95 mode with the AMPS interferer 71dB above wanted signal.

V. CONCLUSIONS

The presented receiver architecture is a first step towards a fully configurable RF front-end. Shifting analog functionality to the DFE enables reconfiguration of receive channel bandwidth and selectivity. The introduction of the DFE fully exploits the advantages of RF-CMOS, which is slowly becoming the main semiconductor technology for RFICs aimed at wireless applications. However, the proposed receiver structure is still limited to predefined frequency ranges. Tunable band-pass filters would be a means to further extend the frequency agility of the analog RF receiver section. Unfortunately, currently available band-pass filters do not meet the demands in terms of tuning ranges, insertion loss, selectivity, power consumption and cost.

ACKNOWLEDGEMENTS

This work is related to the EU funded project E^2R. The authors would like to acknowledge the contributions of their colleagues from the E^2R consortium.

REFERENCES

[1] J. Mitola III, "Software Radios: Survey, Critical Evaluation and Further Directions" IEEE Communications Magazine, May 1995.

[2] A. Springer, L. Maurer, R. Weigel, “RF System Concepts for Highly Integrated RFICs for W-CDMA Mobile Radio Terminals”, IEEE Transactions on Microwave Theory and Techniques, Vol. 50, No. 1, January 2002, pp. 254-267.

[3] H. Kim, H. Lee, H. Choi, J. Park, J. Bu, K. Lee, "A Thermally Driven Tunable TFBAR Bandpass Filter" 34th European Microwave Conference Digest, 2004 pp. 491-494.

[4] P. Smole, W. Ruile, C. Korden, A. Ludwig, E. Quandt, S. Krassnitzer, P. Pongratz, "Magnetically Tunable SAW-Resonator" IEEE International Frequency Control-S Digest, 2003, pp. 903-906.

[5] K. Saitou, K. Kageyama, "Tunable Duplexer Having Multilayer Structure Using LTCC" IEEE MTT-S Digest, 2003, pp. 1763-1766.

[6] M. Rahman, K. Shamsaifar, "Electronically Tunable LTCC Based Multi-Layer Filter for Mobile Handset Application" IEEE MTT-S Digest, 2003, pp. 1767-1770.

[7] G. Kraus, C. Goldsmith, C. Nordquist, C. Dyck, P. Finnegan, F. Austin A. Muyshondt, C. Sullivan, "A Widely Tunable RF MEMS End-coupled Filter" IEEE MTT-S Digest, 2004, pp. 429-432.

[8] T. Burger, Q. Huang, "A 13.5mW 185-Msample/s ΣΔ-Modulator for UMTS/GSM Dual-Standard IF Reception", IEEE Journal of Solid-State Circuits, vol. 36, No.12, pp.1868-1878, Dec. 2001.

[9] R. van Veldhoven, “A Tri-Mode Continuous-Time ΣΔ-Modulator with Switched Capacitor Feedback DAC for a GSM-EDGE/CDMA2000/UMTS Receiver”, IEEE International Solid-State Conference, Digest of Technical Papers, pp. 60-61, 2003, Feb. 9-13, San Francisco, USA

[10] T. Ueno, T. Itakura ”A 0.9 V 1.5 mW continuous-time Delta-Sigma modulator for WCDMA”, IEEE International Solid-State Conference, Digest of Technical Papers, pp. 78-79, 2004, Feb. 15-19, San Francisco, USA

[11] K. Philips et. al., ”A 2 mW 89 dB DR continuous-time Sigma-Delta ADC with increased immunity to wide-band interferers”, IEEE International Solid-State Conference, Digest of Technical Papers, pp. 86-87, 2004, Feb. 15-19, San Francisco, USA

[12] E. Hogenauer, “An Economical Class of Digital Filters for Decimation and Interpolation”, IEEE Trans. On Acoustics, Speech, and Signal Processing, Vol. ASSP-29, No. 2, Apr. 1981

[13] L. Gaszi, “Explicit formulas for lattice wave digital filters”, IEEE Trans. On Circuits and Systems, Vol. CAS-32, No. 1, Jan. 1985