A 900MHz CMOS RF Transceiver Including Digital Baseband and Hardware-MAC for IEEE 802.15.4/ZigBee™ Applications

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Abstract — **This paper presents a fully-integrated RF transceiver operating from 860 to 930 MHz. The device parameters are compliant to the IEEE 802.15.4 standard. The analog portion of the chip contains a direct-conversion receiver, a fractional-N PLL, a direct-conversion transmitter and a TR-switch. Digital baseband signal processing as well as MAC support are also implemented on the same chip. Only minimal external components are needed to form a complete wireless network application - two low-cost crystals, the PLL loop filter, an antenna and a low-cost 8bit microcontroller. Therefore, this chip is one of the most integrated 802.15.4 transceiver ICs presented to date. The input sensitivity is better than -100dBm. The chip is fabricated in a 0.25um CMOS technology with MIM-capacitors, deep n-well and a thick top metal layer.**

I. Introduction

There are many wireless applications that do not require the data rate of systems like Bluetooth (1MBit/s) or WLAN (1 to 54MBit/s). Furthermore, such systems would simply be excessive in terms of power consumption, complexity and cost. It is generally desired to employ systems having performance parameters that are close to the application requirements to conserve power and silicon area, and therefore cost.

For such wireless applications, a standard was developed by the IEEE [1]: "The IEEE 802.15 TG4 was chartered to investigate a low data rate solution with multi-month to multi-year battery life and very low complexity. It is operating in an unlicensed, international frequency band." Potential applications are home and industrial automation, wireless sensors, interactive toys, smart badges and remote controls. The scope of the task group was to define the physical layer (PHY) and the media access controller (MAC). The standard has been available since 2003 [2]. An overview of the specification can be found in [3] and [4]. The definition of the higher protocol layers up to the application profiles is organized by the ZigBee™ Alliance [5].

Since cost is one of the driving factors, a single-chip approach has been chosen. CMOS is the preferred technology to integrate both analog circuitry and high gate count digital circuitry at low cost. With a single-chip CMOS design, the challenge is to achieve good RF performance.

A previous paper of the author [6] already described the architecture and circuit implementation of the main RF and analog blocks of an IEEE 802.15.4 compliant IC along with measurement results of the first revision silicon. This paper will explain a high-frequency related issue in detail that was discovered and analyzed in this IC, namely DC offsets in the direct conversion receiver. Furthermore, the paper will provide an update on the system architecture and present more recent test results.

II. System Overview

Fig. 1 shows the block diagram of the system. The IC contains a 900MHz physical layer (PHY) and a portion of the media access controller (hardware-MAC). The remaining MAC functions (software-MAC) and higher protocol layers up to the application layer are executed on an external 8 bit microcontroller.

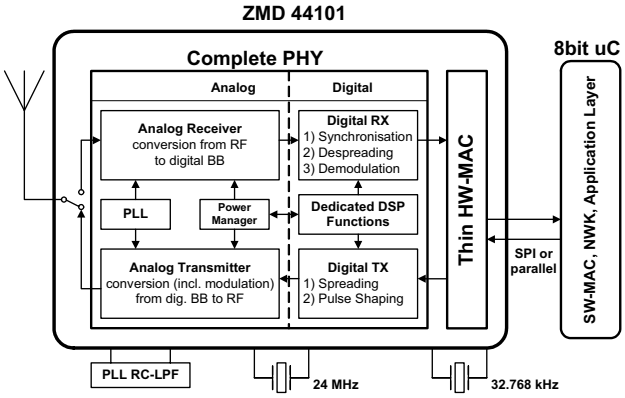

Fig. 1 System block diagram

A. Physical Layer (PHY)

The IEEE 802.15.4 standard defines two different PHYs, one operating at the 2.4GHz ISM band with a data rate of 250kbit/s and one operating at 900MHz [3]. The 2.4GHz band operates worldwide while the 900MHz band operates only in North America and Europe. Therefore, there is one channel at 868.3MHz in the European ISM band with a data rate of 20kbit/s and ten channels from 906 to 924 MHz in the North American ISM band with a data rate of 40kbit/s (see Fig. 5). Both PHYs use Direct Sequence Spread Spectrum (DSSS). The modulation type in the 900MHz band is BPSK. With a PN-code length of 15, this results in a RF bandwidth of 600kHz in Europe and 1200kHz in North America. This IC supports the two 900MHz frequency bands.

All PHY functions are integrated on chip. Only minimal external components are needed to form a complete radio. A low-cost 24MHz crystal is used as a

reference for the PLL and to clock the digital circuitry. To optimize energy consumption in sleep mode while still keeping an accurate time base, a 32.768kHz crystal can be employed. A SAW filter at RF is only required in very hostile RF environments.

The analog portion of the receiver converts the desired signal from RF to the digital baseband. Synchronization, despreading and demodulation are done in the digital portion of the receiver. The digital part of the transmitter does the spreading and baseband filtering, whereas the analog part of the transmitter modulates the shaped baseband signal onto an RF carrier.

B. Media Access Controller (MAC)

The IC contains a portion of the media access controller (hardware-MAC). This relaxes the requirements for the external microcontroller in a network application drastically, in turn allowing the use of a very low-cost device such as an 8-bit 8051.

In order to illustrate the hardware-software partitioning, an example will be used. Beacon tracking and sleep mode are among the features of the HW-MAC. For these functions, as well as for the other hardware features, timers have been implemented on the IC. This allows the device to track beacons autonomously. The IC can also enter sleep mode during the inactive period between longer beacon intervals while still maintaining accurate network timing. The timer allows the IC to wake up autonomously before the next beacon is expected. The current consumption in sleep mode is reduced to 2uA (typical), which enables very long battery life in low duty-cycle applications.

To improve the effectiveness of these two functions even further, a timing correction algorithm has been implemented to account for the natural time base difference between transmitter and receiver. The relation between time base accuracy and average power consumption is described in [7], which is especially important for low duty-cycle applications. After a time drift between consecutive beacons has been detected, the receiver beacon timer is corrected accordingly. This procedure reduces the timing uncertainty when tracking the next incoming beacons and allows even shorter active periods.

III. RF/ANALOG CIRCUIT IMPLEMENTATION

A previous paper [6] already described the architecture and circuit implementation of the three main RF/analog blocks - the direct-conversion receiver, fractional-N PLL, and direct-conversion transmitter. Therefore, the reader is referred to that paper in order to understand that topic in more detail. The following sections briefly summarize the architecture and give typical measurement results.

A. Receiver

The choice of the receiver architecture is mainly a compromise between performance, cost (considering both silicon area and external components), and power consumption [8].

The direct-conversion receiver (DCR) architecture (or Zero-IF architecture) was chosen for this design. This leads to the lowest cost and power consumption solution. However, DCR also has some critical drawbacks, which have to be addressed during design. These include:

- DC offsets from local oscillator (LO) self-mixing
- Even-order distortion (IM2)
- Flicker noise
- LO leakage radiation

The standard applies to burst mode communications. Hence, DC offsets can be reduced with DC offset correction during idle periods. DC offset issues, with possible related problems and their solutions, are discussed in section IV.

Fig. 2 shows the block diagram of the receiver.

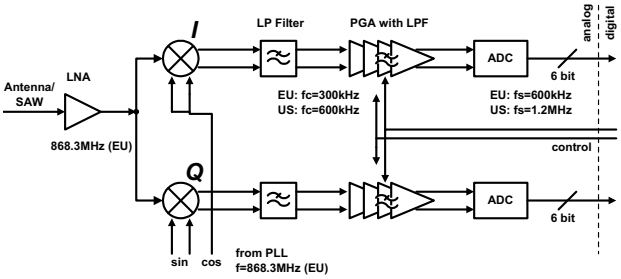

Fig. 2 Direct-conversion receiver block diagram

B. Transmitter

A direct-conversion architecture has been chosen for the transmitter. Fig. 3 shows the block diagram. Since BPSK modulation is used, only one baseband path is required. The design is fully differential. Only the PA output is single-ended. This has the advantage that one RF pin can be shared with the receiver input by using the on-chip RF switch. Furthermore, no external balun is required.

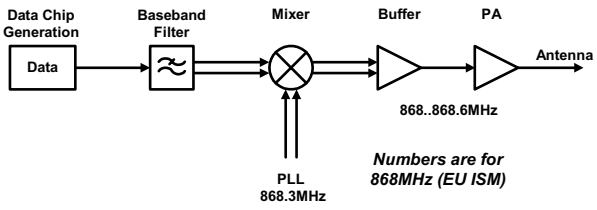

Fig. 3 Transmitter block diagram

The RF path has to be linear to avoid spectral regrowth of the filtered BPSK signal. Two-tone intermodulation simulations have been used to characterize the linearity. Extensive analysis on that type of characterization can be found in [9].

An output spectrum plot is shown in Fig. 4 using a repetitive pn-code as the baseband input, i.e. constant data bits as during the preamble. Though this is not the normal spectrum having random data, it is more suitable to characterize the transmitter parameters.

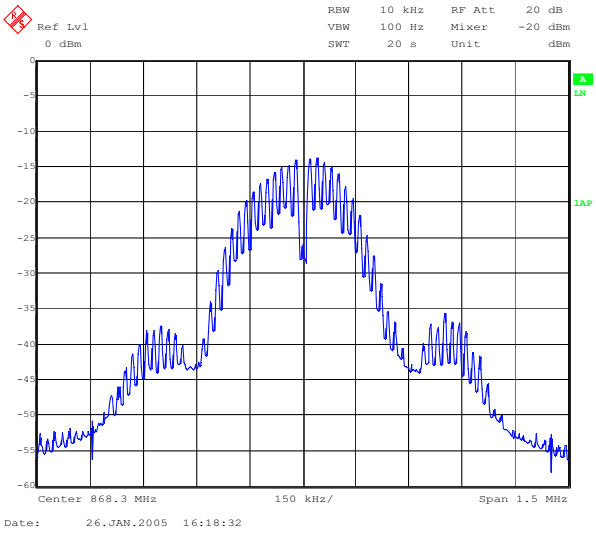

Fig. 4 Transmitter output spectrum

C. PLL

Fig. 5 shows the channel allocation in the 900MHz band of the standard. The goal was to use one PLL for the full band using a fixed crystal frequency, and to have flexibility for future applications with different frequency plans. Therefore, a fractional-N PLL architecture [10] was chosen.

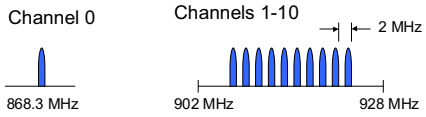

Fig. 5 Channel allocation in the 900MHz band

A double-frequency LC-VCO with IQ-dividers is applied to generate the I- and Q-signals for the mixers. The digital frequency division by two provides a means to generate accurate LO phases. Fig. 6 shows the block diagram of the PLL.

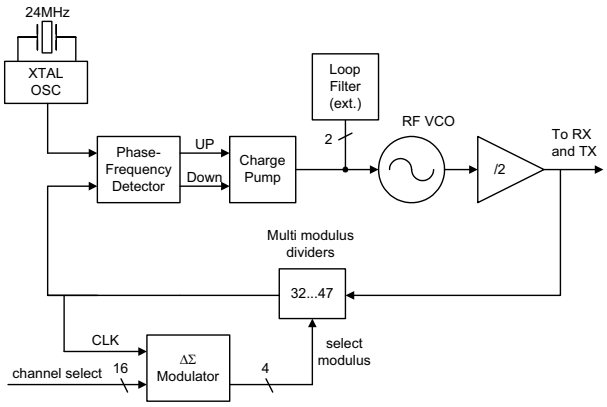

Fig. 6 PLL block diagram

Circuit simulations of the LC-VCO have been conducted together with Matlab simulations of the PLL phase noise behavior. A worst-case VCO phase noise of -89dBc/Hz@100kHz offset (after dividing by two to 900MHz) has been simulated which results in a PLL phase noise of better than -85dBc/Hz from 10 to 100kHz offset.

Measurements have shown a PLL phase noise of better than -80dBc/Hz from 10 to 100kHz offset. That is about 5dB worse than simulation. The difference is mainly due to increased reference phase noise from the 24MHz crystal oscillator since the phase noise at higher frequency offsets does correspond to the simulated values.

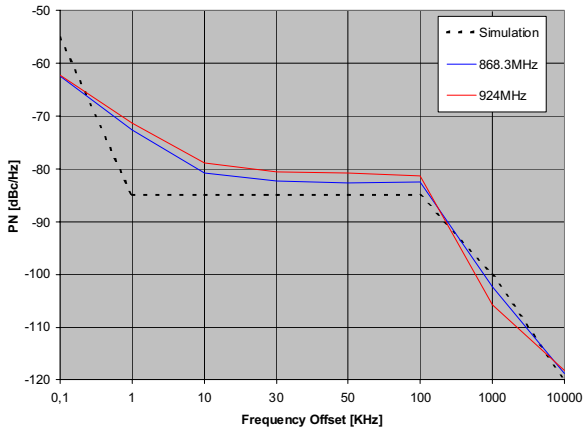

Fig. 7 PLL phase noise measurement for highest and lowest standard channel

IV. DC OFFSETS IN DIRECT-CONVERSION RECEIVER (DCR)

A detailed description of DC offsets has been chosen in order to illustrate possible pitfalls that can occur in RF IC design. Focusing on this design issue does not prevent errors from other sources, but can raise awareness for similar problems.

The DCR architecture is sensitive to DC offsets since the baseband signal spectrum contains considerable energy around Zero. Therefore, DC offsets cannot be easily high-pass filtered without degrading the desired signal.

DC offsets occur for instance by means of LO selfmixing. This effect is shown in Fig. 8. LO-to-RF leakage in the mixer and subsequent reflection of that signal at the LNA output result in an LO component at the RF port of the mixer. The mixing of that signal with the original LO signal having the same frequency causes a DC offset. In an IEEE 802.15.4 system, this offset can be considered static with respect to one reception period because the maximum frame length is defined to be 50ms. Note that this offset might change over time or temperature resulting into a variable DC offset. However, these time constants are considerably longer than one frame length.

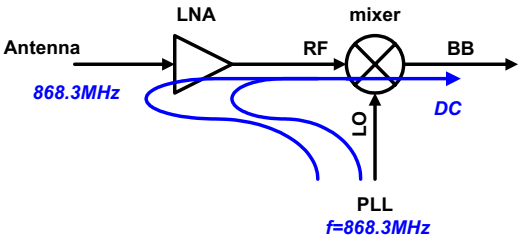

Fig. 8 LO selfmixing on system level

Such DC offsets are typically in the millivolt (mV) range at the output of the mixer, but after considerable gain in the following baseband amplifiers, they can saturate these stages. Therefore, an initial DC offset correction has been implemented in every stage after the mixer. During the correction period, the antenna is disconnected by the on-chip switch, so as to prevent RF signals from disturbing the offset correction.

The LNA output reflection coefficient has to be very similar between the states with antenna switch on and off. A considerable difference would lead to a change of the DC offset after the antenna switch is closed again. These parameters were carefully analyzed and the implementation was found to be feasible.

Laboratory evaluation of a test chip, however, has shown that a considerable change in DC offset - up to about 1mV measured at the output of the mixer - still occurs after the initial DC offset correction when the antenna switch is closed again. This offset change even occurs when no RF signal is applied. Therefore, other factors beyond those previously considered must be described, as outlined below.

The change in DC offset occurs because of the combination of the following effects. First, the mixer does not only leak the LO signal to the RF port, but also to other circuit nodes like power and ground. To model this correctly, one has to introduce finite device mismatches in the differential mixer circuitry, and use a realistic power supply representation instead of an ideal power and ground connection. Second, the LNA uses the same power supply pins as the mixer. Therefore, the LO leakage via the power supply nodes can also be observed at the LNA. The third cause is illustrated in Fig. 9.

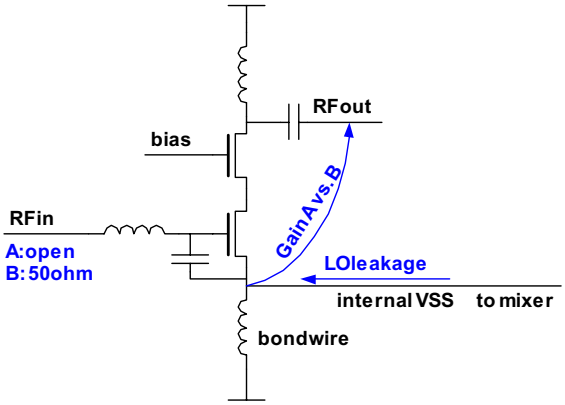

Fig. 9 LNA schematic

Since the LNA is a single-ended circuit, it has only limited power supply rejection. Therefore, a certain amount of the LO leakage signal from the internal ground (VSS) node is transferred to the LNA output. However, this transfer function differs between the two states. In state A, the RF input is open (antenna switch opened), whereas the RF input is connected to a 50ohm impedance in state B. The difference of this transfer function in the two different gate configurations can be understood when the circuit is redrawn as a common-gate amplifier to the LO leakage signal at the source node. The result is a different LO leakage level at the input of the mixer which causes a change of the DC offset as explained in Fig. 8.

In order to reduce this DC offset, each of the individual effects need be reduced. However, there are physical limits (e.g. parasitics, device mismatch) or application requirements (e.g. single-ended LNA, number of power supply pins). Hence, a second DC offset calibration procedure is employed after the initial coarse correction. The calibration has been implemented by means of a DC offset trimming loop. The circuitry preceding the mixer is not changed during this phase.

The conclusion to be drawn from this example is that system level issues need to be carefully transferred to circuit level. Analysis at the circuit level requires comprehensive investigation and modeling of the actual physical circuitry. Yet it is difficult to predict accurate values by simulation when effects like device mismatch and RF leakage are involved. In such cases, either a robust circuit architecture is necessary that provides enough margin by itself, or additional procedures like auto-calibration have to be employed.

V. Experimental Results

Fig. 10 shows a photograph of the chip that has previously been evaluated. The digital portion is located in the upper part of the chip together with the memory blocks. The analog part is divided into the following main blocks (from left to right): receiver baseband, receiver RF, transmitter and PLL. A redesign is currently in progress to fix some issues that were discovered in this silicon in order to obtain production ready silicon.

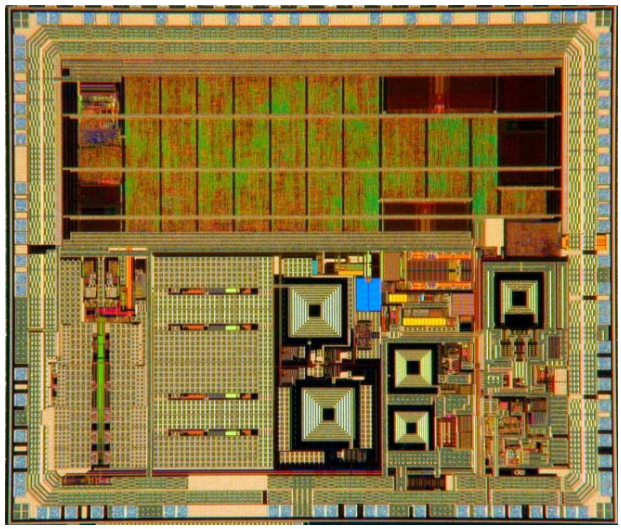

Fig. 10 Chip photograph

The whole chip is functional and has been tested in simple wireless network scenarios. Fig. 11 shows a photograph of the RF module that has been used for laboratory evaluation. A board with socket has also been employed in order to measure several parts quickly. As expected, the RF performance is slightly degraded when using a socket. In addition, a huge influence on the 24MHz crystal oscillator startup time was also

experienced because of the following reason. The two oscillator pins that are connected to the external crystal are located beside each other. The mutual inductance between these pins introduced by the socket reduces the open loop gain drastically. That results in an increased startup time by a factor of three when using the socket.

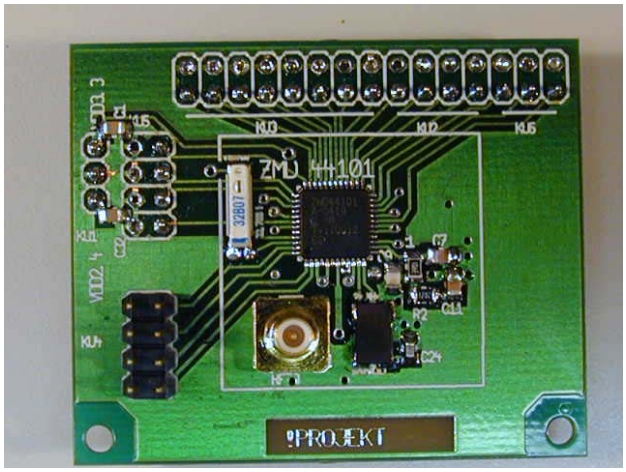

Fig. 11 RF module

The receiver system sensitivity was limited by the DC offset, as explained in the previous section, to about -85dBm@PER<1% (PER - Packet Error Rate). However, the benefits gained by use of the DC offset trimming loop were also measured using test support control software to remove residual offsets. A sensitivity of -100dBm@PER<1% was obtained.

The PER test setup is defined by the standard [2]. Since error detection (CRC) but no error correction is used, a bit error results in an error of that packet. However, the PER test also takes into account packets that are completely missed because of improper synchronization.

Extended temperature testing has been conducted. The device was shown to be functional over the whole temperature range from -40 to 85°C including worst-case supply voltage and process deviation.

A RF ESD protection scheme based on [11] was implemented in the IC. ESD testing has been done using the HBM stress setup. The RF pins have been very carefully evaluated. A protection value better than 2kV was reached for all pins.

V. Conclusion

This paper has presented a fully-integrated 900MHz CMOS RF transceiver. The device parameters are compliant to the emerging IEEE 802.15.4 standard. Using the example of DC offsets in the receiver, it has been shown that the RF CMOS design requires both the understanding of system level effects as well as their careful investigation and modeling at circuit level.

TABLE I
Main IC Parameters

Parameter	Value
Supply voltage	2.2 to 2.7V (typ. 2.4V)
Temperature range	-40 to 85°C
Frequency range	860 to 930MHz
RX current	13mA
TX current	18mA
PLL current	13mA (incl. LO-buffers)
Sleep mode current	2uA (typical)
RX sensitivity	-100dBm
RX input IP3	-20dBm
RX input IP2	+25dBm
TX output power	0dBm (to 50ohms)
PLL frequency resolution	800Hz
PLL phase noise	below -80dBc/Hz@10-100kHz
Package	48-pin QFN (=MLF)
ESD Protection	>2kV HBM
Process Technology	0.25um CMOS, MIM, deep n-well, thick top metal

References

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