Wideband High Dynamic Range Surveillance

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Abstract

In recent radio-communication applications, receivers may be jammed by high power unwanted signals. In this case, the received signal can be considered as the sum of a strong unwanted signal and a very weak target signal. Even though the two signals don't overlap in the frequency domain, the processing of the weak signal becomes very hard as it can be vanished at the output of the Analog Digital Convertor. To avoid this scenario, many nonlinear circuits are proposed in the literature. Our study focuses on the separation of a weak and a very strong signals which are wideband signals and they are very close in the frequency domain. Several circuits have been implemented and simulated. The proposed circuit diagram is also presented. Finally, simulations are presented and discussed.

Index Terms: Dynamic range, AGC, Logarithmic Amplifier, OFDM, electronic warfare, EM surveillance, Radio Cognitive.

1. Introduction

In many modern applications such as tracking radar, electronic warfare, cognitive radio, electromagnetic surveillance, the receiver can be very close to an undesirable transmitter. The latter transmitter can be authorized or unauthorized and it can be transmitting intentionally to jam our receiver or not. The unwanted transmitted signal is considered hereinafter as a jamming signal. In this case, the received signal becomes the result of a very strong unwanted signal (the jamming signal) transmitted by the nearby transmitter and a very weak target signal. In major radio communication applications, authorized transmitters have a limited transmission power. Even though, the ratio between the jamming signal and the signal can be over 80dB. By definition, the dynamic range of a system is the ratio between the smallest and largest signals that can be processed by that system.

An Analog to Digital Convertor (ADC) [1] of 14 to 16 bits is commonly used in digital radio communication receivers. For such ADC, the quantization step can be approximated by the ratio between the maximum input voltage and 2^n, where n stands for the bit number. The quantization step characterizes the dynamic range of our devices.

Indeed, the maximum dynamic range (D_r) reached in a digital system can be approximated by $D_r \approx 20log(2^n) \approx 90dB$, when $n = 15$. In order to limit the dynamic range of the inputs, Automatic Gain Control loops (AGC) have been introduced in several radio-communication receivers. However, the latency of the AGC becomes a major drawback of these circuits in some applications such as the Moving Target Indicator (MTI) radars. The dynamic range of the AGC is also limiting for other applications: radars, fiber-optic communication, and recent radio-communication applications. We should also emphasis the fact that AGC can only adjust their gain with respect to a mono-component signal, starting reference value which is usually the power of the single signal that is need to receive.

To solve the high dynamic range problem, Woronocow and Corney [2] introduced a logarithmic amplifier based on twin-stages. The twin-stages were implemented using two different amplifiers, the first one had high gain and a low limiting output voltage and the second one had a unit gain with high limiting output voltage. Using the circuit developed in [2], Loesch in [3] developed another circuit to perform a logarithmic amplifier over 60dB of dynamic range and it can operate at a center frequency of 768MHz. Loesch's circuit used Avantec UA404 amplifiers. More than a decade later, a "true logarithmic amplifier" was introduced in [4] for radar Intermediate Frequency (IF) applications using monolithic bipolar transistors. According to Barber and Brown in [4], logarithmic amplifier can assist in separating target signal from undesired signals as "the clutter" caused by raindrops. As the phase information is important for MTI radars, the logarithmic amplifier was introduced at the IF stage of the receiver. It is worth mentioning that the proposed logarithmic amplifier in [4] can handle over 80dB of dynamic input range at 70MHz. Using a cascade of six stages and a monolithic Gallium Arsenide Metal–Semiconductor Field Effect Transistor (GaAs MESFET) technology, Smith in [5] developed an integrated circuit to realize a logarithmic amplifier with a 70dB of dynamic range. The major advantage of the Smith's circuit comparing to the one presented previously in [4] is that the new circuit can cover a wide bandwidth between 0.5 up

to 5 GHz. Smith's circuit contains seven FET's, 29 GaAs resistors and 18 capacitors. Holdenried *et al.* in [6] developed a new true logarithmic amplifier using parallel-summation topology. Their circuit has 40dB dynamic range but it can cover the bandwidth DC-4GHz. Their circuit which has low group delay distortion is suitable for use in fiber-optic or radar applications with narrow pulse widths. In [7], Holdenried and Haslett proposed another circuit to cover larger bandwidth, DC-6 GHz; their new circuit uses Silicon-Germanium Heterojunction Bipolar Transistors (SiGe HBT). Their amplifiers use Cherry-Hooper gain stages with emitter follower feedback. In [8], the authors analyzed several solutions and circuits to perform a dynamic range compression, such as: AGC, Voltage controlled Amplifiers (VCAS) circuits and Logarithmic Amplifiers.

In our applications, the dynamic range can be up to 120dB, the signals are considered as wide-band signals (5~80MHz), our device should be able to deal with Very High Frequency (VHF) signals (3 to 30 MHz), Ultra High Frequency (UHF) signals (300MHz – 3GHz) as well as wifi signals (2.4 and 5 GHz). In the following sections, several circuits have been considered and simulated. The above mentioned circuits and other technologies [9-10] and [15] have been considered in our study.

2. Mathematical Model

Let $r(t)$ denotes the received signal and $r_1(t)$ is the signal at the output of the front end, see Fig 1. Let $s_i(t)$, $i = 1$ or 2, stands for the first (the jamming) signal respectively the second (the weak and target) signal filtered by the corresponding transmission channel and received at the receiver's antenna. The relationship between $r_1(t)$ and $s_i(t)$ is given by equation (1):

$$r(t) = s_1(t) + s_2(t) + b(t) \qquad (1)$$

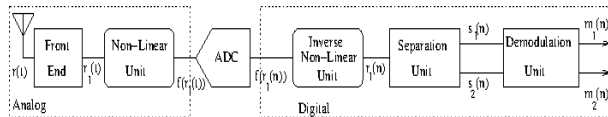Here $b(t)$ is a zero-mean additive white Gaussian noise (AWGN).

Fig 1: General Structure

To increase the dynamic range of the receiver, a non-linear unit (NLU) is introduced in the general structure. The output of the NLU is the signal $f(r_1(t))$. The later signal is converter to a digital signal using an Analog to Digital Converter (ADC). By introducing an Inverse Non-Linear Unit (INLU), the digital version of the received signal can be given by the following equation:

$$r(n) = s_1(n) + s_2(n) + b(n) \qquad (2)$$

Finally a separation unit followed by a demodulation unit should allow us to demodulate separately the two signals.

3. Background & State of the Art

To build the NLU, one can use several possible solutions. In this section, major tested circuits and main ideas developed in our study are discussed.

3.1. PN Junctions

In order to obtain a Log function, one can use a simple circuit based on one or multiple diodes [11-14]. Indeed, the relationship between the current I (in A) and the voltage V (in V) of a diode in forward bias mode is given as follows, [11]:

$$I = I_s \left(e^{\frac{V}{\eta V_T}} - 1 \right) \qquad (3)$$

where the saturation current I_s is given in A, the emission coefficient η depends on the used material ($1 \leq \eta \leq 2$, for germanium $\eta = 2$; for silicon $\eta = 1.3$), the thermal voltage $V_T = kT/q$ (in V), Boltzmann's constant $k = 1.38*10^{-23}$ (in J/°K), the temperature T (in Kelvin, i.e. °K) and the electron charge $q = 1.6*10^{-19}$ C.

3.2 MOSFET

By using a Metal Oxide Semiconductor Field Effect Transistor (MOSFET), one can obtain another nonlinear function as a second order polynomial function. Indeed, the Drain current and Drain voltage relationship is written as follows, [11-15]:

$$i_D = k'_n \frac{W}{L} \left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2 \right] \text{ (Triode region)} \quad (4)$$

$$i_D = \frac{1}{2} k'_n \frac{W}{L} (v_{GS} - V_t)^2 \text{ (Saturation region)} \qquad (5)$$

Where v_{Gs} is the voltage between the gate and the source of the MOSFET, the threshold voltage V_t depending on the MOSFET ($0.5 < V_t < 10$), the process transconductance parameter $k'_n = \mu_n C_{ox}$, the capacitance per unit $C_{ox} = \varepsilon_{ox} / t_{ox}$, the permittivity $\varepsilon_{ox} = 3.45*10^{-11}$ F/m, t_{ox} is the thickness ($t_{ox} = 2$ to 50 nm), the channel length $L = 100$-3000 nm, the source width $W = 200$ nm – 0.1 mm, and n is the surface mobility.

3.3. Bipolar Junction Transistors

Another possible solution can be based on the BJT, as in the saturation mode, the current of through the common can be approximated as follows [11]:

$$i_C \cong I_S \exp\left(\frac{v_{BE}}{V_T} \right) - \left(\frac{I_S}{\alpha_R} \right) \exp\left(\frac{v_{CB}}{V_T} \right) \qquad (6)$$

Where I_s is the saturation current and it depends on the used materials and the dimensions of the BJT, V_T is the thermal voltage, α_R = Common-Base current gain, v_{CB} = voltage between Common and Base and v_{BE} = voltage between Base and Emitter. According to [4], the technique based on diodes is mainly used to produce logarithmic amplifiers for frequency less than 60MHz.

3.4. Multistage Cascade True Logarithmic Amplifier

This technique was introduced firstly by Woroncow and Croney [2] and it shows good results in high frequency, [4] and [6]. The true logarithmic function is achieved by putting in cascade N dual-gain stages. Each stage is composed by a follower and an amplifier which has a gain A, an input saturation voltage V_{IL} and an output saturation voltage $V_{OL} = A\,V_{IL}$, as show in the figure 2.
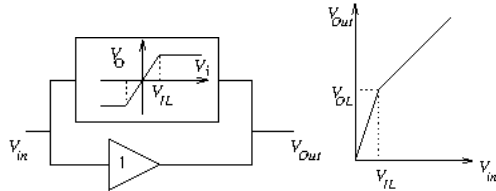

Fig 2 : a) Structure of a stage b) Transfer function a stage

The function transfer of each stage is given as follows:

$$V_{Out} = \begin{cases} (1+A)V_{in} & \text{if } |V_{in}| < V_{IL} \\ (|V_{in}| + V_{OL})\text{Sign}(V_{in}) & \text{ifnot} \end{cases} \quad (7)$$

To explain the main idea, let us consider that the input signal V_{in} is small enough to pass through the (m-1) first stages without exceed the saturation point. In this case, the input signal V_{m_In}, which is the output signal of the previous stage, and the output signal V_{m_Out} of the mth stage are given by:

$$V_{m\_In} = (1+A)^{m-1}V_{in} \overset{\text{Saturation}}{\Longrightarrow} V_{m\_Out} = (1+A)^{m-1}V_{in} + V_{OL} \quad (8)$$

As the saturation is reached at the mth stage, we can conclude that:

$$V_{IL} = V_{m\_In} = (1+A)^{m-1}V_{in} \Rightarrow m = 1 + \log_{(1+A)}\left(\frac{V_{IL}}{V_{in}}\right) \quad (9)$$

The output of the final N stages becomes:

$$V_{Out} = (N-m)V_{OL} + V_{m\_Out} = (N-m+1)V_{OL} + V_{IL}$$

$$= \left(N-m+1+\frac{1}{A}\right)V_{OL} = \left(N+\frac{1}{A} + \log_{(1+A)}\left(\frac{V_{in}}{V_{IL}}\right)\right)V_{OL} \quad (10)$$

To implement the "true log amp", the authors of [6] built their circuit using MOSFET, because it can operate at very high frequency. Each stage contains four amplifiers with different functions. In our study, we realized the true function using the circuit presented in Figure 3. According to [4] the dynamic range of this circuit is $(A+1)^N$. To reach a dynamic

range of 70dB, one can set the parameters of the circuit as follows: A=3.0, V_{OL}=0.764 and N=6. The value of V_{OL} was selected using a heuristic study. It is worth mentioning that the amplifier with the gain and the saturation function has been realized using two different circuits: An amplifier with a gain A followed by a limitation device. The limitation is implemented using two saturated amplifiers, as shown in Figure 4.
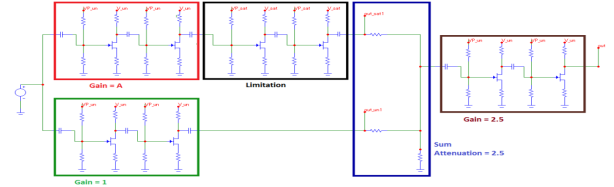

Fig 3: Circuit of one stage of the "true log amp".
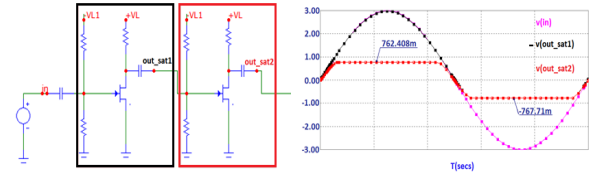

Fig 4: a) Limitation Device b) A saturated sin wave

3.5. Parallel Summation logarithmic amplifiers

To realize a DC-4GHz true logarithmic amplifier, the authors of [6] proposed two other topologies of the true logarithmic amplifier presented in the previous sub-section, see figure 5: A progressive-compression parallel-summation logarithmic amplifier and a parallel-amplification parallel-summation logarithmic amplifier. According to [6], the function of the two circuits presented in Fig. 5 and the original one presented in Fig 4 are the same. However, the sequentially summing and buffering of the original circuit are replaced by parallel summing.
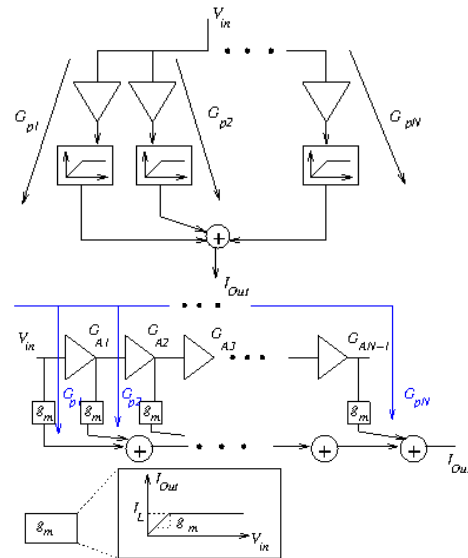

Fig 5: a) Progressive compression parallel-summation b) parallel-amplification parallel-summation

The circuit shown in Fig 5-b exhibits high symmetry among the paths but his dynamic range is low. However, the phase and the group delay matching are improved. Because of the similarity between the two circuits presented in Figure 5, we consider only the transfer function of the progressive compression parallel-summation logarithmic amplifier. Let G_{pi} be the gain of the ith path, as shown in Fig 5-a and G_j be the total gain after the ith stage, $\forall 1 \leq j \leq N$, we can write:

$$I_{Out} = \left(N + \log_A \left(\frac{g_m(A-1)V_{in}}{I_L A^2} \right) + \frac{A}{A-1} \right) I_L \qquad (11)$$

By assuming that the lowest gain path $G_1 = G_{p1} = g_m$ and the saturation amplifier of each stage has the same gain g_m and the amplifiers have the same gain A, one can conclude that $\forall 1 \leq j \leq N$:

$$G_j = g_m A^{j-1} \qquad (12)$$

Using equations (11) and (12), the path gains can be written as follows, $\forall 2 \leq i \leq N$:

$$G_{pi} = g_m A^{i-2}(A-1) \qquad (13)$$

According to Figure 5-a and equation (13), we can conclude that, $\forall 1 \leq j \leq N$:

$$G_{pj} = g_m \prod_{i=1}^{j-1} G_{Ai} \qquad (14)$$

The transfer function of this topology can be evaluated using a similar approach to the one developed in subsection 3.4. Indeed, let us consider that the input signal V_{in} is small enough to pass through the $(i-1)$ first stages without exceeding the saturation point. In this case, the input signal V_{in} is given by:

$$V_{in} = \frac{I_L}{G_{pi}} = \frac{I_L}{g_m A^{i-2}(A-1)} \Rightarrow i = \log_A \left(\frac{I_L A^2}{g_m(A-1)V_{in}} \right) \qquad (15)$$

Where I_L is the limitation current presented in Figure 5-a. As the saturation is reached at the ith stage, that means all the following stages should be saturated and the final output current is given by the following equation:

$$I_{Out} = (N-i)I_L + G_i V_{in} = (N-i)I_L + \frac{G_i I_L}{G_{pi}}$$
$$= (N-i)I_L + \frac{g_m A^{i-1} I_L}{g_m A^{i-2}(A-1)} = \left(N-i+\frac{A}{A-1} \right) I_L \qquad (16)$$

Using equations (15) and (16), we can conclude that:

$$G_j = \sum_{i=1}^{j} G_{pi} \qquad (17)$$

According to [6], the main disadvantage of the progressive-compression amplifier is that the phase delays of all paths are different. Using the Cherry-Hooper stage for all gain stages, the authors of [7] manage to improve the original design and to get approximately the same delay on the different paths.

4. Simulation Results

The main objective of our project consists in the separation of two wideband signals with a high dynamic range. To test the capacity of our circuit, we implemented the structure presented in Figure 1. The nonlinear unit in that structure is achieved using various circuits presented in previous sections. However, the results presented and discussed hereinafter are mainly based on the circuits illustrated in Figures 2, 3 and 4. To illustrate the effect on Ultra-wideband (UWB) signals, we run our simulations using two OFDM signals as transmitted signals [16]. The received signal satisfied the model presented in section 2. In our structure, the ADC converts the analog nonlinear version of the signal to a nonlinear digital signal as shown in the first figure. At this stage, the two signals are still non accessible because of the nonlinear function. For this reason, we introduced in the digital part of our receiver an inverse function, see figure 2. This inverse unit cancels the effect of the nonlinear function and the output digital signal becomes the sum of the two signals as given by equation (2). In order to demodulate the two signals, a separation unit is realized using the circuit shown in figure (5).
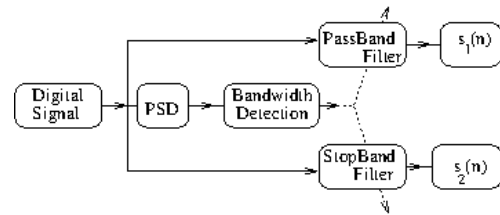

Fig 5: A separation unit.

The real parts of two OFDM signals generated by MATLAB [16] were applied to the circuit simulated in the MICROCAP. The advantage of MICROCAP is that it can simulate analog and digital signals. The digital signals were processed according to equation (18). This equation can inverse the effects of the nonlinear function as discussed earlier, see figure 6:

$$V_{alog} = \left(\frac{V_L}{A} \right) (A+1)^{\left(\frac{V_{log}}{V_L} - N - \left(\frac{1}{A} \right) \right)} \qquad (18)$$
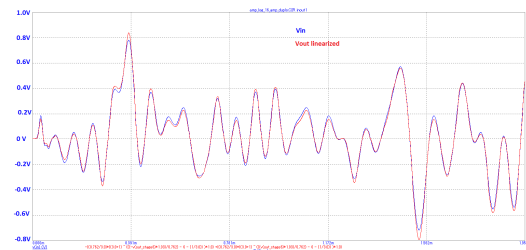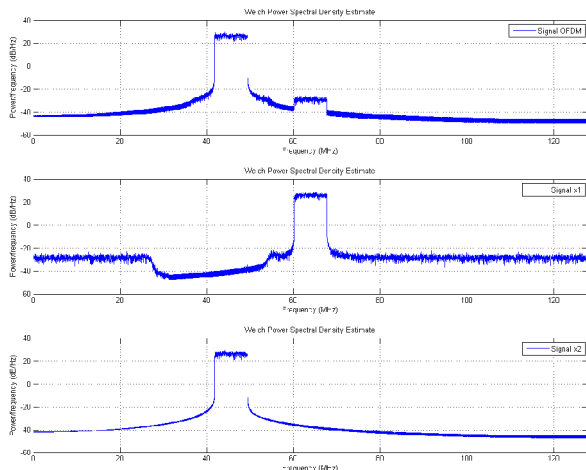

Fig 6: OFDM Signals: the original signal presented in blue and the processed one in red.

It is obvious that the application of the nonlinear function in the analog part of our circuit and its inverse in the digital part can generate nonlinear artifacts. These artifacts can deteriorate the performance of our receiver and increase the Bit Error Rate (BER).

Fig 7: Two OFDM signals separated in the digital part of our circuit.

Finally, using MATLAB, two OFDM signals were generated: a very powerful and a very weak one with 70dB difference between them, see figure 7. The signals were closed in the frequency domain. These signals have been added and introduced to our simulated circuit. Figure 8 shows the received signal and the separated ones at the output of our circuit.
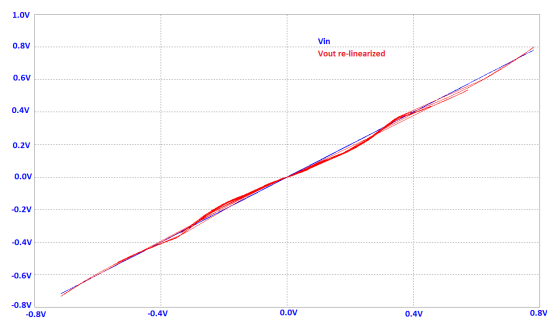
Fig 8: Difference between original and processed OFDM signals

5. Conclusion

Our study consists on the separation and the demodulation of two wideband analog signals with a high dynamic range. In order to digitally process our signals, a nonlinear unit is introduced before the ADC to avoid the vanishing of the weak signal by the ADC. A survey on major logarithmic amplifiers is presented. Various circuits and topologies were tested. To solve our problem by separating and demodulating the mixed signals at the input of our receiver, we proposed a general structure based on hybrid Analog/Digital units. The nonlinear analog function, i.e. the logarithmic amplifier at the analog part of our receiver, is canceled using a digital function in the digital part. The linearized received signals are applied to a separation unit. At the output of the separation unit, the two separated signals are demodulated. Our simulation results corroborate the proposed circuits.

6. References

[1] J. A. Wepman, "Analog-to-Digital Converters and their applications in radio receivers", IEEE Communications Magazine, pp. 39-45, May 1995.

[2] A. Woronocow and J. Croney, "A true I. F. logarithmic amplifier using twin-gain stages", Radio Electronics, vol. 32, N 3, pp. 149-155, September 1966.

[3] B. Loesch, "A UHF true logarithmic IF. amplifier", IEEE Trans. on Aerospace and Electronic Systems, vol. AES-9, N 5, pp. 660-664, September 1973.

[4] W. L. Barber and E. R. Brown, "A true logarithmic amplifier for radar IF applications," IEEE J. Solid-State Circuits, vol. SC-15, pp. 291–295, June 1980.

[5] M. Smith, "A 0.5 to 4 GHz true logarithmic amplifier utilizing monolithic GaAs MESFET technology," IEEE Trans. Microwave Theory Tech., vol. 36, pp. 1986–1990, Dec. 1988.

[6] C. D. Holdenried, J. W. Haslett, J. G. McRory,R. D. Beards,and A. J. Bergsma, "A DC–4-GHz True Logarithmic Amplifier: Theory and Implementation", IEEE J. Solid-State Circuits, Vol. 37, pp. 1290-1299, October 2002.

[7] C. D. Holdenried and J. W. Haslett, "A DC–6GHz, 50 DB Dynamic range, SiGe HBT True Logarithmic Amplifier", International Symposium on Circuits and Systems, Vol. IV, pp. 289-292, Vancouver, Canada, May 23-26, 2004.

[8] W. Kester, J. Bryant, B. Clarke, and B. Gilbert, "SECTION 3 RF/IF SUBSYSTEMS", Analog Devices.

[9] "Gallium Arsenide PHEMT RF Power Field Effect Transistor", Reference MRFG35003N6AT1 Rev. 2, Freescale Semiconductor Technical Data.

[10] 0.5–6 GHz Low Noise Gallium Arsenide FET, data sheet, Hewlett Packard.

[11] Sedra & Smith, "Microelectronic circuits", Oxford, 5th edition.

[12] N. Syorey, "Electronics: A system Approach", Prentice Hill, 2006.

[13] S. Burns and P. Bond, "Principles of Electronic circuits", PWS Publishing, 1997.

[14] T. Bogart, "Electronic Devices and Circuits", Prentice Hall, 1997.

[15] AN-311 Theory and Applications of Logarithmic Amplifiers, SNOA575B, A report of Texas Instruments, www.ti.com/lit/an/snoa575b/snoa575b.pdf, April 2013

[16] M. A. Ingram, G. Acosta, "OFDM Simulation Using Matlab", August 2000