WIDEBAND SPECTRUM SENSING FOR COGNITIVE RADIO

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ABSTRACT

In this work we propose a wideband spectrum sensing system based on hybrid filter banks. The polyphase implementation of the digital counterpart of the filter bank can be modified to include a parallelized version of discrete Fourier transform algorithm (FFT) avoiding this way any sampling rate expanders. In this work we show how to incorporate the FFT block in the structure in order to estimate the wideband frequency contents of the signal. The proposed structure is particularly suitable for FPGA based implementations.

***Index Terms*—** Hybrid Filter Banks, FFT, Spectrum Sensing.

1. INTRODUCTION

Spectrum Sensing is one of the key features that a Cognitive Radio (CR) must have. In the original concept presented by Mitola in his highly cited works [1, 2], the CR must be aware of the spectrum availability in order to find usage opportunities and exploit them to transmit. This concept has gained special attention during the last years due to the increasing demand for wireless communications and the lack of free spectrum to accommodate new services. Traditionally, the spectrum has been allocated in a rigid way and as several studies have shown, most of it is not occupied even in urban areas [3]. One way to solve this problem of spectrum scarcity is to use realtime databases where users can trade spectrum. Another possibility is to perform spectrum sensing in real-time searching for spectrum holes opportunities for transmission. With this strategy, the owners of the spectrum transmit whenever they wish while secondary secondary users transmit when the channel is free. The secondary users must perform the spectrum sensing in real-time in order to avoid collision, or at least to minimize it to acceptable levels of interference.

Several methods have been proposed to perform spectrum sensing and deal with the problem of the low power of the received signals quite difficult to detect in the presence of background noise. The proposed methods goes from basic energy detectors using bandpass filters to cyclostationary signal analysis taking advantage of some prior information regarding transmitted signals [4]. However, most of the proposed methods assume the spectrum is organized in fixed channels with relative narrow bandwith. However this strategy is not useful for a real-time wideband spectrum sensing as it is case of the cognitive radio concept. Some authors recognize this problem and proposed completely new approaches based on the Compressed Sensing concept such as the analog-to-information converter proposed by Tropp *et al.* [5] and the modulated wideband converter proposed in [6]. However, those methods are only efficient if the spectrum is characterized by a fixed level of sparsity. If the sparsity level it is not known a priori, those methods can fail. Moreover, with the expected spectrum occupancy by cognitive radios, the sparsity level is expected to turn unknown. In this paper we propose a different approach using a Hybrid Filter Bank (HFB) front-end where the input RF signal is splitted in M different band-pass channels before being sub-sampled [7]. Then, a digital synthesis filter bank will perform the signal reconstruction by canceling the amplitude and phase distortion and the aliasing terms introduced by the sub-sampling. If the synthesis filter bank is implemented using an efficient polyphase structure, we get at the output M signals with a sampling frequency M times lower than the Nyquist frequency. This format is quite convenient to implement parallel algorithms for spectrum estimation as we will show in this work. This parallelized structure is well adapted to be implemented in FPGA making possible to perform real-time spectrum estimation for RF signals with a large bandwidth. This characteristic is quite important for Cognitive Radios to sense the spectrum and find opportunities in real-time. This work is organized as follows, in the next section we will present the HFBs and the related theory and the main results. On section 3 we will present the spectrum sensing problem for wideband signals. We will end this section with our method that uses a HFB and a parallelized FFT based structure. Finally we have the conclusions.

2. HYBRID FILTER BANKS

Hybrid Filter Banks are a kind of multichannel sampling where the analog input signal is filtered by a bank of analog

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filters, in our case, bandpass filters. In [8] Papoulis have shown that this multichannel sampling, where the input signal $x(t)$ is filtered by M filters $H_k(j\Omega)$ is equivalent to the traditional sampling if the determinant of a square matrix dependent of the filters frequency response and the M aliases components is different from zero for all the frequencies Ω (radians per second). In the Fig. 1 we can see the proposed structure where the filters $F_k(z)$ are the M digital synthesis filters. From the system architecture of Fig. 1, we can write

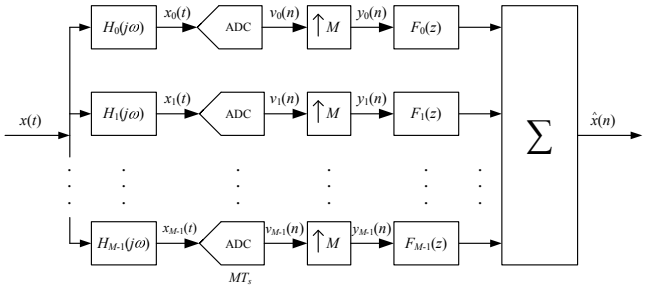

Fig. 1. Generalized structure of the Hybrid Filter Bank.

the Fourier transform of the output signal

$$\widehat{X}\left(e^{j\omega}\right) = \frac{1}{MT_s}\sum_{p=-\infty}^{+\infty} X\left(j\frac{\omega}{T_s} - j\frac{2\pi p}{MT_s}\right) \sum_{m=0}^{M-1} H_m\left(j\frac{\omega}{T_s} - j\frac{2\pi p}{MT_s}\right) F_m\left(e^{j\omega}\right), \tag{1}$$

with ω the angular frequency in radians. Without loss of generality we can assume that the input signal $x(t)$ is low-pass with bandwidth $B < f_s/2$, and so we can define $\widetilde{H}_m\left(e^{j\omega}\right)$ as the periodic extensions of the analog filters $H_m(j\Omega)$. This way we can define an all digital equivalent filter bank where the output signal can be written as

$$\widehat{X}\left(e^{j\omega}\right) = \frac{1}{MT_s}\sum_{p=0}^{M-1} \widetilde{X}\left(e^{j\left(\omega-\frac{2\pi}{M}p\right)}\right) \sum_{m=0}^{M-1} \widetilde{H}_m\left(e^{j\left(\omega-\frac{2\pi}{M}p\right)}\right) F_m\left(e^{j\omega}\right) \tag{2}$$

We can transform the previous equation on a system of equations by sampling the equation in the frequency domain in Q points and getting

$$\mathbf{f} = (\mathbf{H_Q}\mathbf{A})^{+}\mathbf{B}, \tag{3}$$

where $\mathbf{H_Q}$ is a $QM \times QM$ matrix function of the analog filters, $\mathbf{A}$ is a $QM \times ML$ matrix with the discrete Fourier transform terms, $\mathbf{B}$ is the desired frequency response of the system given by

$$B\left(e^{j\omega_q}\right) = MT_s\left[e^{-j\omega_q d}, 0, \ldots, 0\right]^T, \tag{4}$$

and $\mathbf{f}$ is an array with the L coefficients of each digital synthesis filter [9].

2.1. HFB Design

If the number Q of frequency sampling points is large, the system of equations 3 is difficult to solve and some suboptimal algorithms can be used [10]. If the signal $x(t)$ has a sparse support in the frequency domain, it is possible to exploit this to relax the filters $F(z)$ by allowing amplitude distortion and aliasing for the frequencies where the signal $x(t)$ is zero or irrelevant. In [11] the authors used a weighting function to improve the reconstruction results of the HFB and in [7] the author used the Papoulis-Gerchberg algorithm to obtain similar results.

2.1.1. Sensitivity to the analog filters variation

When using the methods based on a priori measurement of the analog filters, we need a perfect characterization of the frequency response of the analog filters in order to design a digital synthesis filter bank that can perfectly compensate the amplitude and phase distortion while perform the cancelation of the aliasing terms due to the subsampling. However, as shown in [10] if the frequency response of the filters are measured off-line, then, when the filters are connected to the final acquisition system, the conditions change and this diference can compromise the reconstruction results of the signal $\hat{x}(n)$ resulting in a limited effective number of bits (ENOB) for the reconstructed digital signal. To solve this problem, several authors [12–14] proposed an adaptive digital synthesis filter bank, but all of them assume that a time interleaved versions of the signal $\hat{x}(n)$ is available to act as the desired signal, which in real implementations can be difficult to obtain. Other authors also proposed some blind techniques [15, 16] to avoid the generation of the desired signal and propose adaptive techniques that only use the output signal from the synthesis filter bank.

2.1.2. Jitter sensitivity

In a HFB with several filters covering a large bandwidth, for the filters with the highest central frequency, two problems arise, i) the higher quality factor needed for this filters and ii) the higher subsampling ratio needed makes the sample and hold operation more sensitive the clock jitter. In [10] the authors proposed a HFB with two stages that can solve this two problems. However the proposed solution is more complex and needs some further developments and study.

2.2. Efficient Implementation of HFB

The structure of the Fig. 1 is not efficient because the interpolators introduce zeroes into the sequences and simultaneously

change the sampling rate by a factor M. Firstly, the sampling rate expanders by a factor M before the digital filters $F_k(z)$ would be a waste of resources. It is well known that a polyphase structure will be preferable. The main advantage of this structure, as we can see in the Fig. 2, is that the interpolators were moved to the output of the filter bank. Consider the polyphase decomposition of the $m-th$ synthesis filter

$$F_m(z) = \sum_{l=0}^{M-1} z^{-(M-1-l)} R_{lm}(z^M) \tag{5}$$

that can be written in matrix form as

$$\begin{aligned}&[F_0(z) \dots F_{M-1}(z)] = \\ &\quad \left[z^{-(M-1)} z^{-(M-2)} \dots 1\right] \times \\ &\quad \times \begin{bmatrix} R_{0,0}(z^M) & \cdots & R_{0,M-1}(z^M) \\ R_{1,0}(z^M) & \cdots & R_{1,M-1}(z^M) \\ \vdots & \ddots & \vdots \\ R_{M-1,0}(z^M) & \cdots & R_{M-1,M-1}(z^M) \end{bmatrix}\end{aligned} \tag{6}$$

where we have now a matrix $\mathbf{R}(z^M)$ with the M^2 polyphase filters $F_m(z)$. This structure is more efficient but combining all the different phases $x_m(n)$ to obtain the signal $\hat{x}(n)$ can be an insuperable task even for the high-end FPGAs. Suppose, for example, that we have a system with $M = 8$ ADCs working at a sampling rate of 100Msps. Then, the sampling rate for the signal $\hat{x}(n)$ would be 800Msps, which is far above the maximum that current FPGA technology can achieve.

The main idea and propose of this paper is to show that it is possible to directly use the polyphase signals x_i in the algorithms of the receiver such as spectrum sensing.

In this work we show that is possible to avoid the generation of the signal $\hat{x}(n)$ if the reception algorithms are modified to use directly the signals $x_i(n)$. Doing this, we have a parallel processing structure that uses the M phases of the signal $\hat{x}$ from the hybrid filter bank, making possible to implement this kind of SDR using a FPGA. Moreover, we will show in the next section how we can modify the FFT algorithm to get a spectrum analyzer for spectrum sensing with wide bandwidth and a high dynamic range at the same time.

3. SPECTRUM SENSING WITH HFB

One of the key features for a cognitive radio is the ability to sense the spectrum in order to find spectrum holes. However, this task must be performed in real-time as the transmission opportunities can be temporary. The spectrum analysis must also be performed for a wide bandwidth. In practice, these two conditions are difficult to meet. The traditional way to perform spectrum sensing for a large portion of the spectrum is based on a heterodyne radio, scanning the spectrum one slice at a time. This technique can not be considered a real-time sensing of the spectrum. One of the most promising spectrum sensing techniques is the multitaper method with

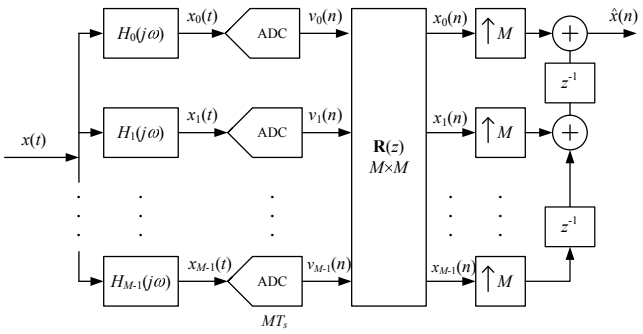

Fig. 2. Generalized structure of the Hybrid Filter Bank.

energy detectors at each frequency output. This method does not need any a priori information about the input signal and due to this can be considered as an agnostic spectrum sensing technique. In [4] the authors show that similar results can be achieved with a properly designed filter bank. To implement a filter bank with a high computational efficiency, we need an efficient implementation of a FFT. In the next section we will see how to take advantage of the parallel architecture of the HFB to implement a parallel version of the FFT that can fulfill the goals of a real-time spectrum sensing for cognitive radios.

3.1. Wideband Spectrum Sensing with HFB

From the Fig. 2 we can see that the last stage of the polyphase implementation of the SFB is nothing more than a M to 1 time multiplexer. If we want to perform spectrum sensing of the signal $\hat{x}(n)$ using the spectrogram with energy detection at each output, the first step is a serial to parallel operation that is equivalent to a 1 to N demultiplexer. However this structure is not well suited for a FPGA implementation. In [17] the author presents a decimated in frequency FFT algorithm, where a N-point FFT is decomposed in 4 $N/4$-point FFTs followed by a 4-points FFT. This decomposition allows the implementation of a larger FFT with a parallelized architecture while taking advantage of the existing FPGA FFT blocks. However, in our case we need a different version of the algorithm where the input signals are a polyphase decomposition of $\hat{x}(n)$. Consider the following definition of the discrete Fourier transform (DFT)

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk} \tag{7}$$

with $W_N = e^{-j\frac{2\pi}{N}}$. We can decompose the signal $x(n)$ in its M phases and the DFT can be written as a function of this signals

$$X(k) = \sum_{n=0}^{N/M-1} \sum_{a=0}^{M-1} x(Mn+a) W_N^{(Mn+a)k}, \tag{8}$$

and if we define the polyphase signals $x_a(n) = x(Mn + a)$ with $a \in [0, 1, \ldots, M-1]$, then we can write

$$X(k) = \sum_{a=0}^{M-1} \sum_{n=0}^{N/M-1} x_a(n) W_N^{(Mn+a)k}. \quad (9)$$

However, we want to transform the N-point DFT in N/M M-point DFTs. To achieve this we can split the Fourier transform vector in M parts as follows

$$X(l + bN/M) = \sum_{a=0}^{M-1} \sum_{n=0}^{N/M-1} x_a(n) W_N^{(Mn+a)(l+bN/M)} \quad (10)$$

where $k = l + bN/M$ with $l \in [0, 1, \ldots, N/M - 1]$ and $b \in [0, 1, \ldots, M-1]$. Then we can simplify

$$W_N^{(Mn+a)(l+bN/M)} \quad (11)$$

to

$$W_{N/M}^{(Mnl)} W_N^{(al)} W_N^{(abN/M)} \quad (12)$$

where we have used these two properties, $W_N^{ZlN} = 1$ and $W_N^{Zln} = W_{N/Z}^{ln}$ with Z an integer. Then we can simplify (10) to

$$X(l + bN/M) = \sum_{a=0}^{M-1} X_a(l) W_N^{al} W_N^{abN/M}, \quad (13)$$

with

$$X_a(l) = \sum_{n=0}^{N/M-1} x_a(n) W_{N/M}^{nl}, \quad (14)$$

where we have used the property $W_N^{abN/M} = W_M^{ab}$. Applying the following change of variable $\tilde{X}_a(l) = X_a(l) W_N^{al}$ we can write (13) as

$$X(l + bN/M) = \sum_{a=0}^{M-1} \tilde{X}_a(l) W_M^{ab}, \quad (15)$$

which can be interpreted as the M-point DFT of the signal $\tilde{X}_a(l)$. The previous equation can be represented graphically as shown in the Fig. 3. As we can see, we have a parallelized structure that uses N/M-point FFTs making this structure more suitable for a FPGA implementation. The main restriction for this kind of implementation would be the number of resources available and not the speed of the sampling rate to represent the signals.

4. IMPLEMENTATION RESULTS

In this section we will provide some preliminary results of the advantages of the proposed parallelised structure. We will consider two scenarios whit the same number of channels $M = 8$, one where we consider a FFT with 32768 bins

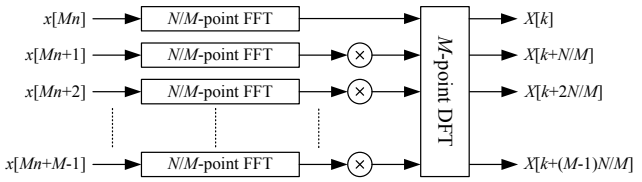

Fig. 3. Decomposition of the N-point FFT in a parallelized version.

and another one with 8 FFTs with 4096 bins followed by the processing showed in the Figure 3. Using Xilinx design suite we implemented the FFT with the LogiCORE IP FFT v8.0 and we get the results presented in Table 1. Both FFTs are

Table 1. FPGA FFT Resources.

Size	Latency	Max. Freq.	DSPs	Memory
bins	μs	MHz	–	18k BRAMS
4096	33	366	120	88
32768	262	235	21	76

Pipelined Streaming I/O type, using 16 bits arithmetic with scaled output. To the results obtained with the 4096 bins FFT we have to consider the matriz multiplication which will use 32 DSP slices of the FPGA to perform the 8×8 complex multiplications at a maximum rate of 440 MHz. Comparing both implementations we can see that our parallelised version needs more DSPs slices and memory but presents a lower latency and can work at higher clock frequency. Moreover, for wider bandwidth systems the proposed architecture scales more easily.

5. CONCLUSIONS

Radio frequency front-ends based on hybrid filter banks are good candidates for cognitive radios. They allow the acquisition and processing of wide-band signals without using high speed ADCs. Moreover, the analog filter bank with several band-pass filters isolate the ADCs from out of band strong noise and allows different gains for different bands improving that way the dynamic range of the whole HFB. With the proposed architecture in this work to perform frequency analysis, we can build a spectrum sensing system for cognitive radio with a high bandwidth working in real-time. This can be used to find spectrum opportunities in real-time for a wide band spectrum.

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