CONTINUOUS TIME DIGITAL SYSTEMS WITH ASYNCHRONOUS SIGMA DELTA MODULATION

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ABSTRACT

Continuous Time (CT) digital signal processing offers several advantages compared to the Discrete Time (DT) approach, while keeping the classical advantages of the latter system. When applying CT Digital Signal Processing (DSP), the signals are digitized in amplitude but processed continuously in time. Since the required chip area for the CT delay lines is quite large, a common way for word length reduction of the CT DSP system input is to apply Delta Modulation (DM). Thus the delay lines must be designed only for a word length of one bit.

In this contribution it will be shown that digitization by Asynchronous Sigma Delta Modulation (ASDM) can result in several advantages for CT signal processing. Using this novel approach the word length of the signal to be processed is also one bit. Nevertheless, compared to the DM system, several advantages such as improved performance and reduced hardware complexity can result.

Index Terms— Asynchronous Sigma Delta Modulator, Continuous Time DSP, Limit Cycle Oscillation

1. INTRODUCTION

In [1] it was shown that a Continuous Time (CT) digital system offers an improved Signal to Noise Ratio (SNR) in the band of interest compared to a Discrete Time (DT) system with the same resolution used for digitization. Since the signals are processed continuously in time, no aliasing occurs and only harmonic distortion is generated by the digitization. In general this results in a smaller noise floor in the band of interest. By using a Delta Modulator (DM), the information is carried on the time axis instead of the amplitude of the signal. DM generates pulses only when the input signal changes and therefore power consumption may significantly be reduced compared to a sampled data system. Furthermore, other advantages of DT digital systems like noise immunity and programmability are inherited.

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The CT Analog to Digital Converter (ADC) which was used in [1], was a DM which basically consists of an N bit quantizer, shift register and other control logic. Fig. 1 shows a DM where $x(t)$ is the input signal and the outputs $c(t)$ and $u/d(t)$ are change and up/down signals respectively. $x(t)$ is quantized in the DM and whenever it changes by one quantization level, a pulse is generated at the output. The signal $c(t)$ consists of these successive pulses, indicating the change of the signal $x(t)$. Furthermore the direction of this change is signaled by $u/d(t)$. These signals are forwarded then to a CT DSP module for further processing.

As there is no clock present in CT digital systems, the signal processing is done asynchronously. Therefore, the delay elements in the CT DSP module are implemented as CT delay lines. The CT delay lines consist of several basic delay cells which store the incoming change and up/down information.

In [2], the granularity time $T_{\mathrm{gran,DM}}$ for a CT DM is determined, which is the minimum distance between two adjacent change pulses when the input signal is a sinusoid. Assuming a sinusoidal input signal with a maximum frequency $f_{\mathrm{in,max}}$ and maximum amplitude A, which is quantized with N bits, $T_{\mathrm{gran,DM}}$ is given by:

$$T_{\mathrm{gran,DM}} = \frac{1}{2^{N-1} \cdot 2\pi A f_{\mathrm{in,max}}} \tag{1}$$

Fig. 2 shows a CT delay line consisting of L cascaded basic delay cells. Each basic delay cell contains a flip-flop for storing the $u/d(t)$ signal and an analog circuit Δ, for delaying the $c(t)$ signal with $T_{\mathrm{gran,DM}}$. The number of basic delay cells required for the implementation of a CT delay line can thus be estimated from $T_{\mathrm{gran,DM}}$. According to (1), if $f_{\mathrm{in,max}}$

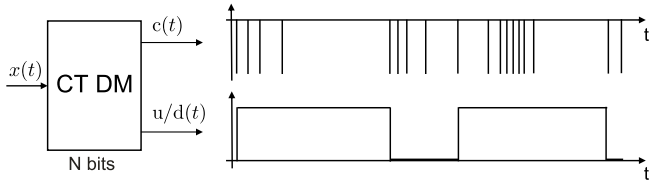

Fig. 1. Change and up/down signals as output of the DM

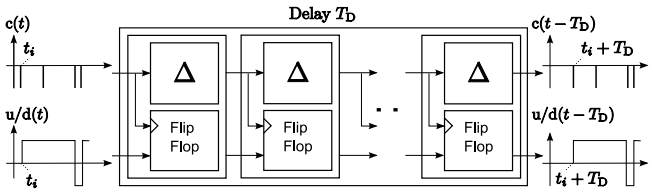

Fig. 2. CT delay line consisting of cascaded basic delay cells

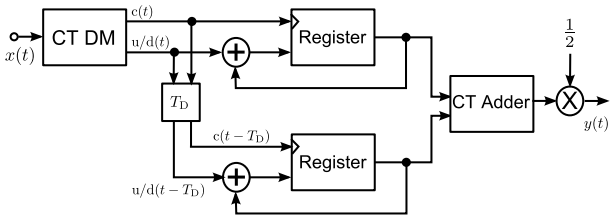

Fig. 3. CT filter structure with DM

is increased, $T_{\mathrm{gran,DM}}$ gets smaller and thus the number of basic delay cells required for the delay elements gets larger. Since we designed our system for audio applications we assumed a maximum input frequency of $f_{\mathrm{in,max}} = 4\mathrm{kHz}$, keeping the implementation complexity in an acceptable range. Of course, the obtained results can also be applied to systems working in different frequency ranges.

The implementation costs of a CT digital system can be optimized by minimizing the number of change pulses per unit time. On the other hand, in-band SNR performance should not degrade much by this optimization. In a DM, the number of change pulses increases linearly with increasing input frequency f_{in}. The N-bit quantizer of the DM introduces some quantization noise which appears as harmonic distortion in the spectrum of the quantized signal. For higher frequencies the in-band SNR improves as the harmonic distortions are shifted out of the frequency band of interest (0 to $f_{\mathrm{in,max}}$).

Fig. 3 shows a simple example of a CT DSP module using one CT delay line with delay T_{D}. The registers with feedback lines are accumulators which reconstruct the modulating signal from $c(t)$ and $u/d(t)$. After addition and 1-bit right shift, the filtered signal is acquired. In the following the Asynchronous Sigma Delta Modulator (ASDM) is introduced as an alternative to DM systems.

2. CT DSP SYSTEMS WITH ASDM

Classical Sigma Delta Modulators (SDM) use oversampling and noise shaping techniques to improve the SNR in the band of interest [3]. ASDM's, in contrary, operate completely in continuous time and require no clock. Their structure is similar to SDM's, but they cannot be modeled anymore as a linear loop where the quantization noise is added as a white noise source. As shown in fig. 4, an ASDM consists of a closed-loop system with a linear filter and a non-linear element. For simplicity a simple integrator is chosen as the linear part. For an actual implementation the ideal integrator can be replaced by a first or second order low-pass filter which limits the gain below the characteristic frequency to a constant value. The 1-bit quantizer is implemented with a hysteresis h and operates as a non-linear element. The output of the ASDM is a periodic square wave [4, 5].

For processing of the ASDM output signal $y(t)$ by a CT DSP system, an additional change signal $c(t)$ must be generated consisting of pulses at the transitions of the square wave. The square wave $y(t)$ can be directly applied to the path for the $u/d(t)$ signal, indicating now high or low level states. Therefore, the filter structure which was used for a CT digital system with DM (fig. 3) can also be used for ASDM signals by removing the accumulation function. This results in reduced implementation costs since the feedback path and registers are not required any more.

ASDM systems introduce no quantization noise to the system since no sampling is performed. Although no clock signal is applied, an unforced periodic oscillation is generated at the output of the closed loop structure in the form of a square wave. This self-oscillation adds extra frequency components to the output spectrum. The instantaneous frequency of this oscillation is called limit cycle frequency. For a constant input signal, the limit cycle frequency takes its maximum value if the input signal is zero and changes with the amplitude of the input signal [5].

In the following, the limit cycle frequency $f_{\mathrm{c}} = \omega_{\mathrm{c}}/2\pi$ will be determined for a system with a zero input signal and an integrator as the linear filter. From [4], the relationship between the transfer function $H_{\mathrm{L}}(\mathrm{j}\omega)$ of the linear filter and the hysteresis h for an ASDM system with input signal $x(t) = 0$ can be described by:

$$\frac{4}{\pi} \sum_{n=1,3,5,\cdots}^{\infty} \frac{1}{n} \mathrm{Im}\{H_{\mathrm{L}}(\mathrm{j}n\omega_{\mathrm{c}})\} = \pm h \qquad (2)$$

The frequency response $H_{\mathrm{L}}(\mathrm{j}\omega)$ of an integrator with the characteristic frequency ω_{p} is given by:

$$H_{\mathrm{L}}(\mathrm{j}\omega) = \frac{1}{\mathrm{j}\omega/\omega_{\mathrm{p}}}$$

Inserting this expression into (2) we obtain:

$$\frac{-4}{\pi} \sum_{n=1,3,5,\cdots}^{\infty} \frac{1}{n} \frac{1}{n\omega_{\mathrm{c}}/\omega_{\mathrm{p}}} = \pm h$$

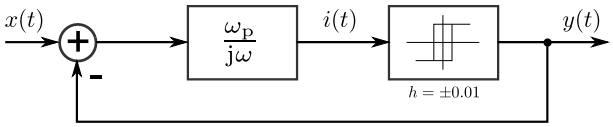

Fig. 4. ASDM closed-loop system

Hence ω_c is given by:

$$\begin{aligned}\omega_c &= \frac{4\omega_p}{\pi h}\sum_{n=1,3,5,\cdots}^{\infty}\frac{1}{n^2} \\ &= \frac{4\omega_p}{\pi h}\frac{\pi^2}{8}\end{aligned}$$

Finally, using $f_c = \omega_c/2\pi$ the limit cycle frequency is:

$$f_c = \frac{\omega_p}{4h} \tag{3}$$

In [5] it was shown that for a non-zero input signal, the limit cycle frequency is lower than the value which is given by (3). If a sinusoidal input signal $x(t) = A \cdot \sin(2\pi f_{in} t)$ is applied, the limit cycle frequency is a function of time:

$$f_{cs}(t) = \left(1 - A^2 \sin^2(2\pi f_{in} t)\right) \cdot f_c \tag{4}$$

Furthermore, The average limit cycle frequency for the sinusoidal signal $x(t)$ is:

$$f_0 = \left(1 - \frac{A^2}{2}\right) \cdot f_c \tag{5}$$

For the sinusoidal input signal, additional distorting frequency components are generated at the output of the ASDM. These components appear around f_0 and can be described by Bessel functions at frequencies $f_0 \pm k f_{in}$, where k is an even integer [5].

From (3) and (5) we conclude that the average limit cycle frequency f_0 of the sinusoidal signal can be reduced by decreasing ω_p and increasing h. The lower limit of f_0 will be determined by the distorting frequency components which are shifted into the band of interest and degrade the in-band SNR. It should be high enough to keep these components out of the band of interest. Furthermore small values of h make the hardware implementation more critical. As shown in [6], a reasonable lower value for h is 0.01.

3. OPTIMIZATION OF A FIRST ORDER ASDM

Since the transfer characteristic of an ideal integrator can be realized only over a limited frequency range, a more realistic first order low-pass filter with the following transfer function was chosen for the simulations:

$$H_L(j\omega) = \frac{1}{1 + j\omega/\omega_p} \tag{6}$$

Fig. 5 shows the power spectrum of an ASDM output signal with hysteresis $h = 0.01$ and characteristic frequency $\omega_p = 15\text{kHz}$, for a sinusoidal input signal of $A = 0.8$ and $f_{in} = 3973\text{Hz}$. As seen in the figure, the noise spectrum increases up to around f_0 and for higher frequencies it decreases again. For sampled modulators, on the other hand, the noise spectrum increases up to half of the sampling frequency where it has its maximum.

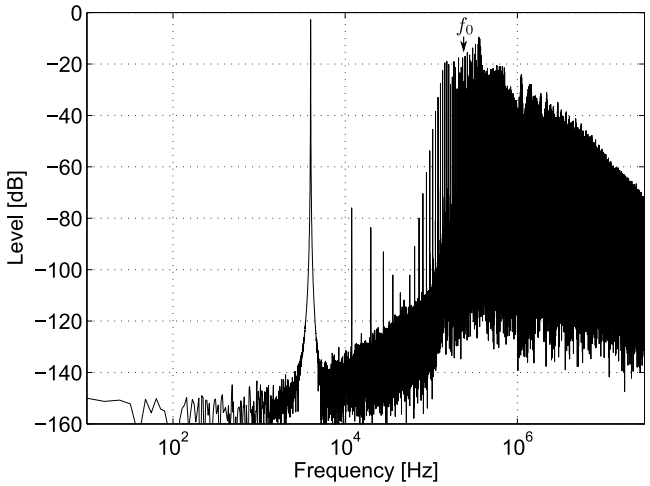

Fig. 5. Power spectrum of an ASDM output signal

For the limit cycle frequency of this first order modulator, equation (3) still holds [4]. Using this relationship the limit cycle frequency for a zero input signal is $f_c = 375\text{kHz}$. Therefore inserting this value into (5), the average limit cycle frequency for the considered sinusoid is $f_0 = 255\text{kHz}$. As can be seen in fig. 5, there are a number of Bessel components around f_0. The frequency band of interest from 0 to 4kHz is however only slightly affected and an in-band SNR of more than 70dB is obtained.

By increasing the characteristic frequency of the low-pass filter ω_p and therewith the average limit cycle frequency f_0, the distorting frequency components diminish from the baseband range and the in-band SNR becomes better. On the other hand, increasing f_0 results in faster unforced oscillation at the ASDM output and thus the pulse rate of the change signal $c(t)$ is increased.

In the following, the performance of an ASDM system with the above parameters is compared with the performance of a DM. All the simulations are performed by Simulink ODE algorithms in CT mode. To make a fair comparison, the in-band Signal to Error Ratio (SER) and the change pulse rates for both systems are taken into account. The in-band SER is calculated as the ratio between the in-band powers of the modulator input and error signals. The error signal is the difference between the input and output of the modulator [7].

Fig. 6 shows the in-band spectra of an ASDM error signal for different input signal frequencies. As can be seen in the figure, the harmonic distortions become larger with increasing input frequency f_{in}. Therefore the in-band SER becomes worse, although the distortion components are shifted out of the band of interest for higher frequencies.

In the diagram in fig. 7, the in-band SER is shown for this type of modulator, where the characteristic frequency ω_p

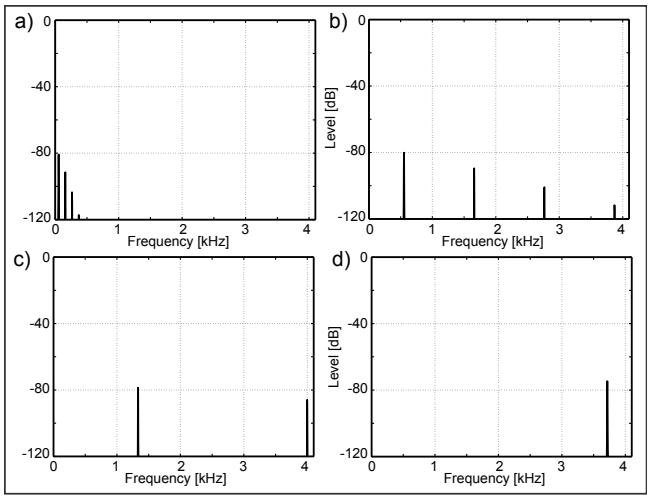

Fig. 6. Power spectra of an ASDM error signal for different input signal frequencies: a) $f_{\rm in} = 53$Hz, b) $f_{\rm in} = 553$Hz, c) $f_{\rm in} = 1333$Hz, d) $f_{\rm in} = 3717$Hz

of the filter and the frequency of the sinusoidal input signal are the parameters. The amplitude has been set to $A = 0.8$. As can be seen in the figure, the in-band SER improves with increasing $\omega_{\rm p}$ and degrades with increasing input frequency $f_{\rm in}$. For $\omega_{\rm p} \geq 15$kHz the SER is better than 70dB for all input frequencies in the range of 0 to 4kHz.

The pulse rate of the change signal $c(t)$ for an ASDM system is constant and does not depend on the input signal frequency. It is obtained from the average limit cycle frequency as follows:

$$R_{\rm ASDM} = 2f_0 < 2f_{\rm c} \tag{7}$$

The maximum rate $R_{\rm ASDM,max} = 2f_{\rm c}$ is obtained when a zero input signal is applied to the system.

In order to achieve about the same performance using a DM system, a quantizer with $N = 10$ bits resolution is required. As seen in fig. 8, the in-band SER is considerably degraded for $f_{\rm in} < f_{\rm in,max}/3$ due to the distortion components falling into the band of interest. For $f_{\rm in} > f_{\rm in,max}/3$, the only in-band distortion component is located at the input signal frequency itself. Since this component is constant for input frequencies $f_{\rm in,max} > f_{\rm in} > f_{\rm in,max}/3$ the SER is also constant in this frequency range.

For a delta modulated signal, the pulse rate of the change signal increases linearly with the input frequency $f_{\rm in}$. Since all $2^N - 1$ quantization levels used by a mid-tread quantizer are crossed two times during one period of a sinusoidal signal with maximum amplitude, the respective maximum pulse rate of the change signal is given by [2]:

$$R_{\rm DM,max} = (2^{N+1} - 4) \cdot f_{\rm in} \tag{8}$$

Using equations (7) and (8) the input frequency $f_{\rm in}^*$ can be determined, for which both systems generate the same number of change pulses per unit time:

$$f_{\rm in}^* = \frac{f_0}{2^N - 2} \tag{9}$$

Thus, for input signal frequencies smaller than $f_{\rm in}^*$ the DM generates fewer change pulses than the ASDM, whereas for frequencies larger than $f_{\rm in}^*$ the ASDM performs better with respect to the pulse rate.

In order to compare the performance of the optimized ASDM and DM systems, a sinusoidal signal with a maximum amplitude $A = 0.8$ is applied to both systems. For DM, a resolution of $N = 10$ bits is used to obtain an SER higher than 70dB. Similarly, as shown in fig. 7, an ASDM with $\omega_{\rm p} = 15$kHz and $h = 0.01$ is required for an SER above 70dB. Using (3) and (5) the average limit cycle frequency is $f_0 = 255$kHz. Inserting this value and $N = 10$ into (9), we obtain 250Hz. Therefore for input signal frequencies above 250Hz, the ASDM generates fewer change pulses and still has an SER higher than 70dB.

In order to suppress the unwanted out of band frequency components, decimation filtering has to be performed at the output of the ASDM system. It is essential that the time distances between the transitions of the ASDM output are preserved during the filter processing. In the classical DT DSP, the required accuracy for the detection of these transitions would result in a very high oversampling rate. When using CT DSP, these time distances are however automatically kept by the CT delay lines with a very high accuracy. A structure for an optimized CT decimation filter was proposed in [8].

The granularity time $T_{\rm gran,ASDM}$ for processing of the ASDM output signal can be determined from the minimum distance between adjacent transitions of the output signal. The input signal $x(t)$ is supposed to be a constant or a sinusoidal signal. The instantaneous duty cycle of the output signal is the ratio of the instantaneous pulse-width $\alpha(t)$ and limit cycle period $T(t)$ [5]:

$$D(t) = \frac{\alpha(t)}{T(t)} = \frac{1}{2}(1 + x(t)) \tag{10}$$

Inserting the instantaneous limit cycle frequency $f(t) = 1/T(t)$ into (10) and solving for $\alpha(t)$ gives:

$$\alpha(t) = \frac{1 + x(t)}{2f(t)} \tag{11}$$

Similar to (4), the limit cycle frequency can be written as $f(t) = (1 - x^2(t))f_{\rm c}$. Inserting this into (11) gives:

$$\alpha(t) = \frac{1}{(1 - x(t))2f_{\rm c}}$$

For a sinusoidal signal with a maximum amplitude A, $T_{\rm gran,ASDM} = \min_t\{\alpha(t)\}$. Therefore the granularity time for processing of the ASDM output signal is given by:

$$T_{\rm gran,ASDM} = \frac{1}{(1 + |A|)2f_{\rm c}} \tag{12}$$

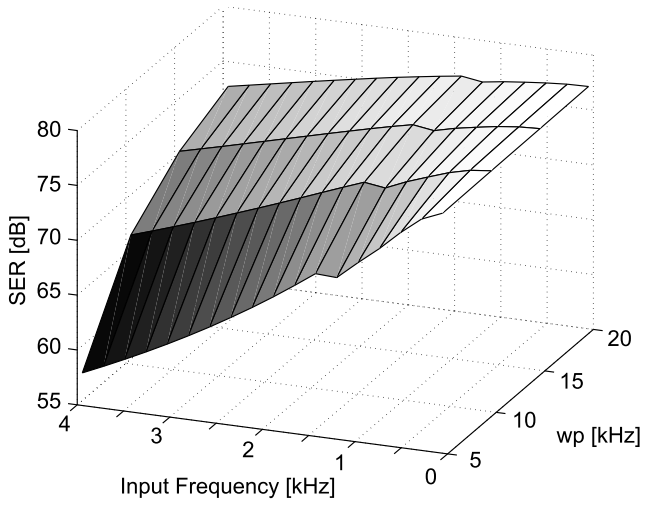

Fig. 7. In-band SER of the ASDM output signal

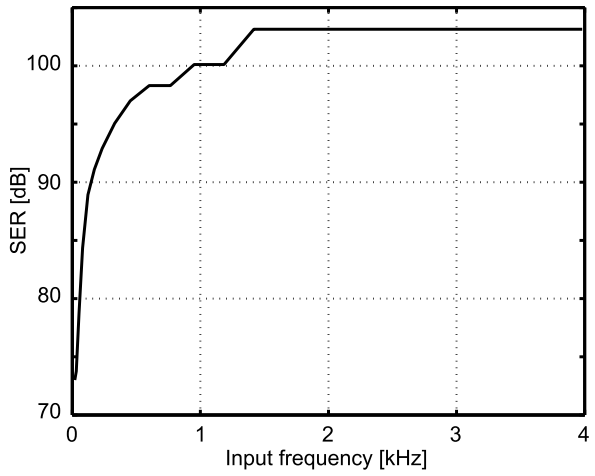

Fig. 8. In-band SER of the DM output signal

It can simply be shown that (12) is also valid for a constant input signal $x(t) = A$.

Thus, with $A = 0.8$ and $f_{\mathrm{c}} = 375\mathrm{kHz}$, a very moderate value of $T_{\mathrm{gran,ASDM}} = 740\mathrm{ns}$ is obtained. From (1) the required granularity for the delay elements using a DM system with $N = 10$ is $T_{\mathrm{gran,DM}} = 97\mathrm{ns}$ which is significantly smaller. Therefore the delay elements for the CT DSP behind the ASDM are simpler and the implementation cost is lower.

In a classical DT SDM system each doubling of the sampling rate results in an improvement of about $9\mathrm{dB}$ for the SNR [3]. Therefore to achieve an in-band SNR of $70\mathrm{dB}$ for the DT SDM output, an oversampling ratio of 140 must be used. For $f_{\mathrm{in,max}} = 4\mathrm{kHz}$, this results in a sampling rate of $1.2\mathrm{MHz}$. Comparing this value with $f_{\mathrm{c}} = 375\mathrm{kHz}$ for the CT ASDM, verifies the superior performance of the latter system.

4. CONCLUSIONS

Due to the kind of signal processing performed in CT digital systems the realization of the respective delay elements is a critical point with respect to the required chip area and the accuracy. In order to reduce the implementation requirements, DM systems had been previously proposed to be used with CT DSP's. In this contribution it was shown that the digitization by an ASDM can result in several advantages.

Compared to DM systems, the pulse rate of the change signal can be reduced for a large range of input frequencies, even though it does not depend on the input frequency anymore. Furthermore, it was shown that decimation filtering behind the ASDM can be performed very efficiently by CT filters since the granularity requirements are reduced and no accumulation is required.

Theoretical fundamentals and design rules for the optimization of the ASDM structures are given. Furthermore, an optimized first order ASDM was presented and compared to a DM system as well as a sampled data system.

5. REFERENCES

[1] B. Schell and Y. P. Tsividis, "A Continuous-Time ADC/DSP/DAC System With No Clock and With Activity-Dependent Power Dissipation", *IEEE Journal of Solid-State Circuits*, pp. 2472-2481, Nov. 2008.

[2] B. Schell, "Continuous-Time Digital Signal Processors: Analysis and Implementation", Ph.D. thesis Columbia University, 2008.

[3] S. Norsworthy, R. Schreier, G. Temes, *Delta-Sigma Data Converters, Theory, Design, and Simulation*, IEEE Press,1997.

[4] S. Ouzounov, E. Roza, J. Hegt, G. Weide, A. Roermund, "Analysis and Design of High-Performance Asynchronous Sigma-Delta Modulators With a Binary Quantizer", *IEEE Journal of Solid-State Circuits*,vol.41,2006.

[5] E. Roza, "Analog-to-Digital Conversion via Duty-Cycle Modulation", *IEEE Transactions on Circuits and Systems*, vol.44, no.11, pp.907-914, November 1997.

[6] P. Wei and T. Hudson, "Performance Improvement of an Asynchronous Sigma-Delta Modulator by Programmable Hysteresis", *WCECS 2009*, SF, USA, 2009.

[7] M.Kurchuk and Y.Tsividis, "Signal-Dependent Variable-Resolution Clockless A/D Conversion With Application to Continuous-Time Digital Signal Processing", *IEEE Transactions on Circuits and Systems*,vol.57,May 2010.

[8] D. Brückmann, K. Konrad and N. Tavangaran, "Delay line adjustments for the optimization of digital continuous time filters", *IEEE ICECS*, Athens, Greece, 2010.