OFDM TRANSCEIVER FOR IEEE 802.20 STANDARDS

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ABSTRACT

Orthogonal Frequency Division Multiplexing (OFDM) is a modulation technique which is now widely used in various high speed mobile and wireless communication systems. In this paper we show the design and implementation of an OFDM transceiver for the IEEE 802.20 standard, featuring a variable length FFT, and targeting a low cost Xilinx® Spartan™ 3A DSP Field Programmable Gate Array (FPGA). The design includes dynamic FFT size, variable length cyclic prefix, and different window combination options to meet the requirements of the wideband Frequency Division Duplexing (FDD) mode of IEEE 802.20. The resources occupied by each part of the design are analysed. The paper also features test and implementation results.

1. INTRODUCTION

The aim of any communication system is to transfer information from one place to another. For many years the conventional modulation techniques used for this purpose have been AM, FM, PM, ASK, FSK, PSK, i.e. single carrier modulation [1]. To increase the data rate and to combat the frequency selective fading in the channel, the multicarrier approach has recently been introduced in a number of IEEE 802.xx and 3G standards. OFDM is a multicarrier modulation technique which is capable of achieving high spectral efficiency in multipath fading channels. OFDM essentially splits the available spectrum into number of narrowband transmission channels known as subcarriers, across which the transmitted data is distributed; the data rate on each subcarrier is therefore at a lower rate. At the receiver, the subcarrier data streams are multiplexed back together to form a single data stream [2]. OFDM finds widespread application in digital audio broadcasting, digital video broadcasting, 802.11, 802.16 and 802.20 standards.

FPGAs are flexible and reconfigurable integrated circuits, whose functionality is programmed by the designer rather than the device manufacturer. Unlike an Application-Specific Integrated Circuit (ASIC), FPGAs can be reprogrammed multiple times, even after deployment. The high speed, parallel architecture provides complete control over the degree of parallelism in the design, and arithmetic wordlengths. This flexibility is a key advantage of FPGAs over traditional DSP processors. Many recent high speed digital signal processing applications such as networking, video and image processing and communications are implemented by using FPGA [2]. This work investigates the efficient FPGA implementation of an OFDM transceiver design for the IEEE 802.20 physical layer. Xilinx System Generator and ISE tools were used to design and implement the OFDM transceiver, targeting the low cost Spartan 3A DSP 1800A device.

2. RELATED WORK

Since the publication of the IEEE 802.20 [12] in June 2008 standard a number of papers have appeared in the literature on both modelling , simulating and implementing the standards. The simulation and analysis of a complete 802.20 are modelled in [3],[4] by using Matlab where an *end_to_end* Reverse Link (from AT to AN) transmitter and receiver are simulation for AWGN and Multipath Rayleigh fading channel models.

A number of other published works address the implementation of general OFDM based systems on FPGAs. In [5], Wouters et al investigate implementation aspects of an OFDM-based wireless LAN modem, together with adaptive configuration of the FPGA. M.Jose Conet [6] deals with the design and FPGA implementation of an Intermediate Frequency (IF) transceiver for the IEEE802.11a OFDM-based standard for Wireless Local Area Networks (WLANs). In [7] and [8], Garcia presents the design, validation and FPGA implementation of an OFDM modulator for IEEE 802.11a and IEEE 802.16 using a high level design tool, and also reports the resources requirements for the developed system. Serra [9] presents a prototype OFDM transmitter using FPGA for the Hiperlan/2 standard (i.e. the European equivalent of IEEE 802.11a). Also, Dick [10] reports on the FPGA implementation of an OFDM transceiver, including receiver synchronization and channel estimation as well as Fast Fourier Transform (FFT)-based modulator and demodulator. The FPGA resource requirements of the various sub-systems are reported and the design methodology employed for system design, verification and

FPGA implementation is described.

However, while all of the above work deals with OFDM implementations in general, they do not consider the IEEE 802.20 standard specifically. Therefore in this paper we present the design and implementation of OFDM transceiver for IEEE 802.20. In particular the work will address issues related to wordlengths, cost efficient implementations, and setting FFT sizes, cyclic prefix lengths and windows included within the standard.

3. THE IEEE 802.20 STANDARD

IEEE 802.20 is a standard for high-speed, reliable, cost effective broadband communication, and includes an OFDM wideband mode and a 625kHz Multi-Carrier (MC) mode. Time Division Duplexing (TDD) is supported by both the 625k-MC mode and the OFDM wideband mode; FDD duplexing is supported by the OFDM wideband mode only [11]. This paper is concerned with the FDD variant of the OFDM wideband mode.

Both the forward and reverse link use OFDM modulation. Transmission on the forward link is divided into superframes, where each Forward Link superframe consists of a preamble followed by a sequence of 25 Forward Link Physical Layer (NFLPHY) frames. The *FDDHalfDuplexTDDPartition* field of the Overhead Messages Protocol defines whether a guard interval is inserted between each of the NFLPHY frames. The alternative structures of an FDD forward link superframe are therefore as shown in Figure 1.

Figure 1 - FDD Forward Link Superframe Structure

Transmission on the reverse link is also divided into units of superframes, with each superframe consisting of a sequence of 25 reverse link PHY frames, and the guard interval defined by the *FDDHalfDuplexTDDPartition* variable. The time corresponding to the forward link superframe preamble is left blank on the reverse link. The structure of an FDD reverse link superframe is shown in Figure 2..

Figure 2 - FDD Reverse Link Superframe Structure

The design presented is this paper specifies that *FDDHalfDuplexTDDPartition* = 1, i.e. that a guard interval is present in each of the forward and reverse links.

The OFDM symbol parameters for the different FFT sizes supported by IEEE 802.20 are given in Table 1, where N_{FFT} is the number of points in the FFT, T_{CHIP} is the duration of a chip, N_{CP} is the number of cyclic prefix, and T_{CP} is the duration of the cyclic prefix. The duration of the windowing guard interval, and the overall symbol, are given by T_{WGI} and T_S, respectively.

Table 1: Forward Link OFDM Symbol Specifications

Parameter	N_{FFT} = 512	N_{FFT} = 1024	N_{FFT} = 2048	Units
Chip Rate $\frac{1}{T_{CHIP}}$	4.9152	9.8304	19.6608	Mcps
Subcarrier spacing $\frac{1}{T_{CHIP}N_{FFT}}$	9.6	9.6	9.6	kHz
Bandwidth of operation	2.5 - 5	5 - 10	10 - 20	MHz
Cyclic Prefix Duration $T_{CP} = N_{CP}N_{FFT}T_{CHIP}$ N_{CP} = 1, 2, 3, or 4	6.51, 13.02, 19.53, or 26.04	6.51, 13.02, 19.53, or 26.04	6.51, 13.02, 19.53, or 26.04	µs
Windowing Guard Interval $T_{WGI} = \frac{T_{CHIP}N_{FFT}}{32}$	3.26	3.26	3.26	µs

Table 1: Forward Link OFDM Symbol Specifications

Parameter	N_{FFT}= 512	N_{FFT}= 1024	N_{FFT} = 2048	Units
OFDM Symbol Duration $T_s = N_{FFT}T_{CHIP} \times \left(1 + \frac{T_{CP}}{16} + \frac{1}{32}\right)$ N_{CP} = 1, 2, 3, or 4	113.93, 120.44, 126.95 or 133.46	113.93, 120.44, 126.95 or 133.46	113.93, 120.44, 126.95 or 133.46	μs

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Figure 3 - Time Domain Processing

$$x(t) = \frac{1}{\sqrt{N_{FFT}}} \sum_{k=0}^{N_{FFT}-1} X_k e^{\frac{j2\pi\left(k-4-\frac{N_{FFT}}{2}\right)(t-T_{CP}-T_{START})}{N_{FFT}T_{CHIP}}} \quad (1)$$

Figure 4 - Overlap and add operation for *EnableHalfDuplex* = 0

Figure 5 - Overlap and add operation for *EnableHalfDuplex* = 1

4. FPGA DESIGN

$$w(t) = \begin{cases} 0 & (t-T_{START}) < -T_{WGI} \\ 0.5 - 0.5\cos\left(\frac{\pi(t+T_{WGI}-T_{START})}{T_{WGI}}\right) & -((T_{WGI} \le (t-T_{START})) < 0) \\ 1 & 0 \le (t-T_{START}) < T_{CP}+T_{FFT} \\ 0.5 + 0.5\cos\left(\frac{\pi(t-T_{START}-T_{FFT})}{T_{WGI}}\right) & T_{CP}+T_{FFT} \le (t-T_{START}) < T_S \\ 0 & (t-T_{START}) \ge T_S \end{cases} \quad (1)$$

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Figure 6 - The Mapper

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Figure 7 - The IFFT Unit

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IFFT output. The cyclic prefix circuit is shown in Figure 8.

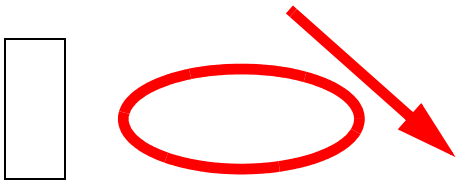

Figure 8 - Cyclic prefix adder circuit

Figure 9 - Window generator circuit

Figure 10 - The demapper circuit

5. RESULTS

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Figure 11 -

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6. DISCUSSION

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Figure 12 -

7. REFERENCES

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