EXPERIMENTS ON DESIGNING LOW POWER DECIMATION FILTER FOR MULTISTANDARD RECEIVER ON HETEROGENEOUS TARGETS

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ABSTRACT

This work presents the results of different experiments conducted on a power-efficient decimation filter design in a wireless multi-standard receiver context. This paper evaluates the efficiency of some low-power solutions applied to the digital filtering domain. This evaluation was done for heterogeneous target devices and for both ASIC and FPGA technologies. With this work, the authors prove that identifying the best low-power solution is very dependent on technology and target device.

1. INTRODUCTION

Software Defined Radio is a promising concept and is expected to be widely employed in the next generations of wireless communication terminals. Multi-standard receivers are a typical application of software defined radio. Indeed, these receivers support different communication standards such as GSM, UMTS, etc. and handle different frequency bands and bandwidths. For these reasons, Multi-standard receivers have to be configurable which is relatively easy to achieve with software defined radio techniques. Most of the receiver's architectures proposed in literature [1,2] use a direct or a low-IF down conversion front-end followed first by an over sampler analog-to-digital converter, then by a decimation selector base-band filter.

Previous works propose several contributions for multi-standard digital filters for decimation and channel selection [3-4]. These contributions aim mainly at reducing the computation complexity and the surface occupation of the decimation selector base-band filter [3]. However, more emphasis has to be put on the low-power design of the base-band filtering processor.

The main objective of this work is to evaluate and compare the efficiency of previously proposed design for low-power filter. This comparison is based on FPGAs and ASICs solutions and intends to identify the adequate techniques for each technology.

This paper is organized as following: Section 2 provides a literature overview of the existing solutions for power reduction at different design levels for CMOS technologies. Section 3 reviews the multi-standard decimation filter architecture. In Section 4, we present low-power solutions used for the filter's power optimization. Section 5, presents implementation results for ASIC and FPGA technologies. Finally, conclusions are given in section 6.

2. POWER REDUCTION TECHNIQUES

Power dissipation in digital CMOS is composed of two major components: static power dissipated by leakage currents and dynamic power essentially due to the circuit activity [6].

Dynamic Power reduction can be implemented at different levels of the design abstraction: system level, algorithmic level, architectural level, gate level and even at the circuit and technologic level. The authors in [6] showed that an important reduction of consumed power can be achieved at each level using specific techniques.

Switching activity can be reduced using different methods and at different levels. The simplest solution consists in reducing the total number of operations. Others solutions use redundant binary representations and operator transformations [7], arithmetic operations optimization [8] (e.g., using the booth or the Wallace multiplier), and the clock gating method [5]. At the circuit level, reducing the glitches reduces the power consumption.

In this work, we detail the low-power solutions implemented for a multi-standard decimation filter on various target technologies. The main objective is to identify the best low power consumption circuit regardless of the technology.

3. DECIMATION FILTER ARCHITECTURE

The decimation filter is used after a 4th order sigma-delta modulator placed in homodyne direct conversion RF front-end transceiver. We have proposed in [3] the Multi-standard receiver architecture for the DECT, the GSM and the UMTS standards. This design was optimized in term of computing complexity for a low cost area implementation. The structure of this receiver is given in (Fig. 1).

Figure 1- Decimation filters cascade structure.

The decimation filter is composed of three filters progressively reducing the frequency rate down to the Nyquist frequency. The first stage is composed of a cascade of Integrator-Comb filter. The second stage is a Halfband filter, known for its low complexity and suitable for decimation by two.

The last FIR filter is programmable depending on handled standard.

4. LOW POWER DESIGN FLOW

In this section we will describe the different low power techniques used in our low power design flow.

4.1 Clock-gating technique

Clocks represent an important source of dynamic power dissipation because of their high switching activity and their long data path. The clock-gating method principle consists of isolating blocks or part of blocks of a given design when they are not used. The block isolation is performed through the disconnection of the clock driving it. Hence, its dynamic power consumption is eliminated and the total power consumption is limited to its static power. Detailed implementation of the decimation filter using clock-gating is given in [5].

4.2 Multiply and Accumulation unit optimisation

In this architecture, in addition to the application of clock-gating technique, the MAC unit implemented in the sub-filters of the two last FIR stages is optimized through the usage of a low-power Multiplication-Accumulation Unit (MAC) [10]. The multiplier used in the proposed MAC unit is split into 3 parts: Partial-Product Generation, Partial Product Summation and finally Carry Propagate Adder (CPA). The Partial-Product reduction step generates the partial products of the multiplication using the modified Booth algorithm in radix-4 base. For the partial products summation, a carry-save addition tree technique based on (m, 2) compressors is used. Result of the partial products summation is two vectors Sum and Carry. This Result is accumulated with previous results using a carry save adder. Finally, a Carry Propagate Adder is used to perform the final addition. It is to highlight that the considered MAC unit works at a frequency rate equal to the double of the rate of MAC it replaces [10].

4.3 Multi-standard filter partitioning

This architecture represents an implementation of the decimation filter where new clock-tree distribution between stages of the filtering chain is used in association with new partitioning of the last stage FIR filter. In fact, the half-band filter uses the polyphase-form implementation and operates at $f_s/2 \times M$; where f_s is the sampling rate at the input of the decimation filter. Since previous stage, composed of the derivator part of the CIC filter, operates at the frequency f_s/M it was possible to generate clock driving halfband filter by sample clock division of the last stage CIC filter's clock.

The FIR selector filter also uses the polyphase-form implementation to operate at $f_s/2 \times 2 \times M$. Hence, we propose to drive the filter with the comb-filter's clock divided by $2 \times 2 \times M$.

On the other hand, we propose to split the last FIR stage into two filters. The new proposed design focuses on the reduction of dynamic power. The first filter handles the UMTS standard and the second filter handles the GSM and DECT standards. This new partitioning is based on the filters' orders. Indeed, the selector filter order of GSM and DECT standard are close. Their orders are almost the double of the order of the UMTS standard selector filter. Because only one stage is used at once, clock-gating technique reduces the dynamic power consumption especially for UMTS standard. The Sub-filters resulting from the polyphase decomposition of the last two stages are implemented using MAC units. In a second approach, all the sub-filters are implemented in their direct form and optimization at the operand level is done for both area and power reduction.

4.4 Hardware operator optimisations

The direct form of the FIR filters uses as many adder and multiplier circuits as the operations required for the filter. Hence, using modified Booth algorithm and Wallace tree reduction techniques increases the operating frequency and reduces the total activity of the decimation filter.

4.4.1 Half band filter partitioning

The half-band filter has been designed to handle three standards using the same coefficients. This feature allows the simplification of the partial products generation in multiplier circuits. The new implementation of the half-band filter uses a mixed radix Booth algorithm. Indeed, depending on the value of the coefficients, the Booth algorithm radix-2 or the Booth algorithm radix-4 can be used to reduce the number of partial products as much as possible. Then, all the partial products generated from the different multipliers are added in a tree structure using the Wallace-tree compressor. The Wallace tree technique delivers output samples in a carry save binary representation. Finally, a carry propagate adder converts the Wallace tree's output to two's complement binary representation [11].

4.4.2 Selector filter partitioning

The selector filter was split into two parallel filters. The first one concerns the UMTS standard only. Hence, its coefficients are fixed. This feature allows the use of the same technique used for the half-band filter. The second filter deals with GSM and UMTS standards; its coefficients are configurable. Then the same approach used for the half band filter cannot be used. We decide then to separate the GSM and DECT selector channel filters. This allows the use of a mixed radix Booth algorithm on the fixed coefficients of the three selector filters and Wallace compressor tree for the addition of partial products addition [11].

5. IMPLEMENTATION RESULTS

5.1 Selected designs

In order to identify the best low power circuit, we have designed 7 architectures for the Multi-standard decimation chain. The description of the low power architectures is given bellow and is summarised in Fig.2.

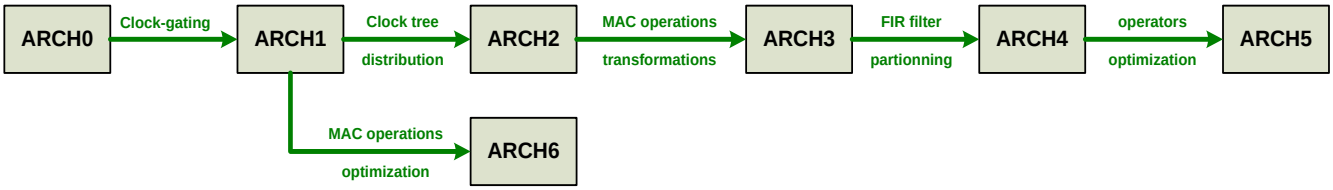

Figure 2- Architectural optimisation flow used to design the low power designs

ARCH0 represents the initial low area implementation architecture [5] of the decimation filter where no power-optimization is applied.
ARCH1 is the implementation based on clock-gating.
ARCH2 represents the implementation where appropriate clock-tree distribution is applied associated with two stages selector filter partitioning and clock-gating. The FIR filters are implemented in their direct-form structure.
ARCH3 represents the implementation based on the appropriate clock-tree distribution associated with two-stage selector filter partitioning and clock-gating. In this architecture, the two last stages' filters are implemented using MAC units.
ARCH4 represents the implementation based on appropriate clock-tree distribution associated with two-stages selector filter partitioning. The FIR filters are implemented in direct form using optimized operators.
ARCH5 represents the implementation based on appropriate clock-tree distribution associated with three-stage selector filter partitioning and clock-gating. The FIR filters are implemented in direct form using optimized operators.
ARCH6 is the implementation based on clock-gating and optimized Multiplication-Accumulation Unit.

5.2 Target technology selection

We implemented the 7 architectures described in section 5.1 on different ASIC and FPGA technologies to evaluate their power efficiency.

Our evaluation approach takes into account the dynamic power consumption as well as the static power consumption. The purpose of target diversification is to evaluate first, the efficiency of power reduction methods used over different devices and technologies and then to measure the gap in terms of area, maximum reachable frequency and power consumption between FPGA and ASIC devices.

We have selected for these experiments two Xilinx FPGA devices, a Spartan 3A-DSP (low cost) and a Virtex 5 (high performance). We have also selected two Altera FPGA with the same features, a Cyclone III (low cost) and a Stratix II (high performance). Finally we have chosen two ASIC technologies, the first one is 90nm ST library 1.26V which provides high performance computation speed and the second one is 65nm ST library 0.90V which providing very low power circuits.
Xilinx Spartan-3A DSP and Altera Stratix II FPGAs are manufactured using 90-nm process technology and VIRTEX-5 and CYCLONE III FPGAs are manufactured using 65nm Process technology.

The power consumptions were measured at 80 MHz using XPower tool for Xilinx FPGA devices, Power-Play tool for Altera FPGA and Design Vision for ASICs.

5.3 ASIC technology results

Experimental results for 65nm and 90nm ASIC technology are summarised in tables 1 and 2, respectively. These tables provide area, critical path delay and static and dynamic power consumption for implemented designs.

Tables 1 and 2 clearly show that all optimized architectures reduce the dynamic power consumption of the filter-chain. However, this dynamic power reduction always comes with a static power increase for ARCH2 and ARCH5 for the two technologies. For 90nm technology, the dynamic power consumption decrease is smaller than the static increase providing a global power increase in both ARCH2 and ARCH5. The static power consumption for ARCH2 is mainly due to the large number of arithmetic operators (multipliers and adders) required in the direct form FIR filters.

In 65nm process technology, all considered architectures reduce the overall power consumption. This is due to the fact that in the selected low power technology, the dynamic power consumption is the dominant part of the total power consumption. If we consider only the dynamic power consumption, the best filter implementation is ARCH4. In fact, for both chosen technologies, the dynamic power consumption was reduced by more than 60%. If we consider also the static power consumption, the best architectures are the ARCH4 for 65nm technology and ARCH1 for 90nm.

The 90nm ARCH1 implementation based on clock-gating optimization provides a dynamic power reduction of 55% and a total power reduction of about 49%. The area was reduced by 22.7%. This result could be explained by the fact that in the selected 90nm process technology static and dynamic powers dissipation is equivalent.

ARCH1 is the best architecture in term of power consumption for the multi-standard filter in this technology since it presents the best compromise between Static/Dynamic powers.

The 65nm ARCH4 implementation is the best low-power implementation candidate since it provides a power consumption reduction of 73,81%. In the same time, this design decreases also the critical path and has almost the same occupied area as ARCH0. Power consumption results could be explained by the fact that in this technology, the static power consumption is low versus the dynamic one.

Architecture	Area (um²)	Latency (s)	D.Power (mW)	S. Power (mW)	Gain (%)
Arch0	96905	3,81	10,64	5,06	--
Arch1	74882	3,67	4,7	3,31	48,98%
Arch2	180456	1,21	9,46	8,55	-14%
Arch3	82440	1,21	5,18	3,67	43,63%
Arch4	89018	1,20	4,13	4,39	45,63%
Arch5	183523	1,20	6,86	9,31	-3%
Arch6	88897	1,20	4,38	4,39	44,14%

Table 1- Implementation results on ASIC 90nm technology 1.26V

Architecture	Area (um²)	Latency (s)	D.Power (mW)	S.Power (mW)	Gain (%)
Arch0	50722	6,25	3,48	0.019	--
Arch1	40300	6,24	1,56	0.014	65%
Arch2	96867	2,97	2,12	0.033	52,14%
Arch3	44105	2,97	1,49	0.015	66,54%
Arch4	49861	2,96	1,16	0.018	73,81%
Arch5	101571	2,96	2	0.038	54,8%
Arch6	47548,3	4,62	1,55	0.018	65,14%

Table 2- Implementation results on ASIC 65nm technology 0,90V

Architecture	Flip-Flop	LUT	DSP	Freq (MHz)	D. P (mW)	S. P (mW)	Gain (%)
Arch0	2239	3409	0	41	513,2	122,1	--
Arch0_DSP	2244	2481	6	43,4	331,7	119,2	29
Arch1	2101	3279	0	66	87,3	114,7	68,2
Arch1_DSP	2101	2441	6	66	93,5	115,5	67,1
Arch2	3859	6315	0	36	55	115,1	73,2
Arch2_DSP	2912	2911	32	34	69,5	115,3	70,9
Arch4	1780	3532	0	46,5	26,3	114,6	77,8
Arch6	2423	4174	0	56,6	82,5	115,5	68,8

Table 3- Implementation results on Xilinx SPARTAN 3A DSP FPGA

Architecture	Flip-Flop	LUT	DSP	Freq (MHz)	D. P (mW)	S. P (mW)	Gain (%)
Arch0	2238	3150	0	107,5	61	304	--
Arch0_DSP	2257	1906	3	140	59	304	0.5
Arch1	2105	3005	0	165,7	65	304	-1
Arch1_DSP	2107	1858	3	165,7	40	303	7
Arch2	3931	6536	0	47	41,2	302,8	6,7
Arch2_DSP	3935	2705	32	60,7	43	303	6,2
Arch4	1902	3087	0	134	26,6	301,9	10,9
Arch6	2423	3231	0	141	11	301	15,4

Table 4- Implementation results on Xilinx VIRTEX5 FPGA

Architecture	Flip-Flop	LUT	DSP	Freq (MHz)	D. P (mW)	S. P (mW)	Gain (%)
Arch0	1941	2475	0	73	553,2	432,8	--
Arch0_DSP	1944	1436	24	79.52	534,9	432,3	1,9
Arch1	1675	2375	0	134,25	368,9	415,3	20,5
Arch1_DSP	1688	1332	24	143.43	354,6	380,7	25,4
Arch2	3680	6546	0	406,5	752,1	384	-15,2
Arch2_DSP	3670	7821	96	419,64	1057	364	-44
Arch4	1665	3599	0	425.17	451,2	382,3	15,5
Arch6	2313	2872	0	68,95	452,7	382,2	15,3

Table 5- Implementation results on Altera STRATIX-2 FPGA

Architecture	Flip-Flop	LUT	DSP	Freq (MHz)	D. P (mW)	S. P (mW)	Gain (%)
Arch0	1941	3035	0	43.53	200,4	153,4	--
Arch0_DSP	1941	2012	12	48,48	169,3	153,5	8,7
Arch1	1657	2886	0	58,58	167,4	125,6	17,2
Arch1_DSP	1657	1863	12	52,68	139,5	88,7	35,5
Arch2	3673	8773	0	244,68	220,4	161,6	-8
Arch2_DSP	2843	3159	123	243,66	308,8	139,6	-26,7
Arch4	1665	3861	0	250	163,1	139,2	13,7
Arch6	2311	3735	0	50,86	175,7	125,8	14,9

Table 6- Implementation results on Altera CYCLONE-3 FPGA

5.4 Results on Xilinx FPGA

Table 3 and 4 provide implementation results respectively on Xilinx Spartan 3A-DSP and Virtex-5 FPGAs.

We notice that for Spartan 3A device, the application of the clock-gating method in ARCH1 reduces drastically the power consumption. The architecture ARCH2 is an efficient low-power implementation since it allows a power reduction of 73,24%. After the optimization of the arithmetic operators in ARCH2 which leads to ARCH4, the power consumption is reduced farther to 77,8%.

We can notice from Table 4 that ARCH6 presents the best power consumption in Virtex-5 FPGA. ARCH6 which is based on clock-gating and optimized MAC unit, provides the best result regarding the dynamic power consumption and therefore the total power consumption (gain of 15,4%). This little gain is due to the heavy amount of the static power consumption contribution.

It is important to underline that the ARCH4 which is the best architecture on Spartan 3A device presents a gain of only 10.9% on Virtex 5. We notice also that Xilinx DSP components are not efficient for low power optimisation as their usages increase the dynamic consumption.

5.5 Results on ALTERA FPGAs

Tables 5 and 6 provide the filter chain implementation results respectively on target Stratix II and Cyclone III Altera devices.

The operators' optimization in ARCH4 and ARCH6 allows power consumption reduction on Stratix II FPGA of 13.68% and 14.93%, respectively. However, ARCH1 which is based only on clock-gating technique shows better power consumption results than all other implementations especially when FPGA DSP blocks are used. These results can be explained by Altera's synthesizer optimization efficiency and from the hardware multiplier power characteristics.

Now, if we consider both frequency and power consumption criteria, ARCH4 is the best implementation since it permits to reach required frequency and save 13.68% of total power consumption.

Clock-gating architecture offers also the best power consumption results on Cyclone III FPGA, allowing 25,42% power consumption reduction. Result explanation is similar to Stratix II one.

5.6 Result analysis

The results discussed in previous section prove that all the optimisations performed from ARCH0 to ARCH6 are not always efficient in term of power reduction.

In fact, ARCH2 on Altera Stratix II shows a power consumption increase even if this same architecture presents better results on all other considerate experiments. This confirms that the power optimisation process for a given design is tightly technology dependant.

Results presented in section 5.5 confirm that in case of FPGAs technology, the static power should not be considered when comparing the different architectures' power consumption. In fact, static power consumption depends more from FPGA circuit's size itself rather than the implemented design.

This can be verified by the results obtained on Spartan 3A DSP and Virtex5 Xilinx FPGAs. Indeed, Virtex5 is supposed to be low-power device but since it is larger than Spartan 3A DSP, it consumes more static power than Spartan 3A DSP.

In ASIC based implementations, the comparison between different architectures should consider both static and dynamic power consumption. We can notice that for the considered 90nm process technology, static and dynamic power consumption contributions are equivalent. We found equivalent results on 65nm process technology. In fact, static and dynamic power consumption contributions were only scaled by the process technology size difference. To eliminate static contribution we used an ultra low power library during the synthetisys process.

The work presented in this paper proves that the power optimisation performance evaluation has a sense only when considering these three aspects: the application context, the optimisation technique, and the target technology. This explains the paradigm of power optimisation for embedded systems.

6. CONCLUSION

The aim of this work was to design a low-power decimation filter for a multi-standard receiver. For this purpose, several implementations of the decimation filtering chain based on low-power implementation techniques were presented. The various architectures obtained during the optimisation steps have been implemented and evaluated on ASIC and FPGA technologies. We have evaluated their power consumption, their area, and their maximum throughput possibility (frequency). Static and dynamic powers were considered during power consumption evaluation. Eventually, we have shown that power consumption optimization is tightly technology dependant.

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