CDTA-BASED QUADRATURE OSCILLATOR DESIGN

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ABSTRACT

In this paper, a quadrature oscillator topology is designed using CDTA (Current Differencing Transconductance Amplifier) based allpass building blocks. Low-voltage CMOS realization of the CDTA element is also given, which is used to implement allpass filters. Resulting circuit is capable of working in supply rails between ±0,75V and total power consumption is just 0,75 mW. SPICE simulation results are supplied to verify the theoretical study.

1. INTRODUCTION

Current Differencing Transconductance Amplifier is first presented in [1] by Biolek, which is then found as a useful active building block for current-mode signal processing and some circuit solutions are given using this active block by several authors. Although it is proposed recently, it is already shown to be a versatile element in several circuits [2-5]. However, to the best knowledge of authors, no CDTA-based oscillator topology exists in the literature. This paper proposes a CDTA-based quadrature oscillator topology. Resulting circuit consists of only six passive elements and two CDTA block which is more compact than its operational amplifier and OTRA counter parts [6-7] and the condition of oscillation is independent of frequency of oscillation. Thanks to low-voltage CMOS CDTA element in the allpass sections, total power consumption of overall topology is 0.75mW and designed oscillator is suitable for single battery operated systems because of its symmetrical ±0.75V power supplies. SPICE simulation results are given to confirm the theoretical study.

2. CDTA

Current Differencing Transconductance Amplifier consists of an input current substractor and dual output transconductance stage. Input stage takes the difference of input signals and transfers this difference current to the intermediate z terminal where this current is converted to voltage via an external impedance. Then, this voltage is again converted to balanced output currents by the dual output transconductance stage. Symbol of the CDTA element is shown in Fig.1 and defining equations are given.

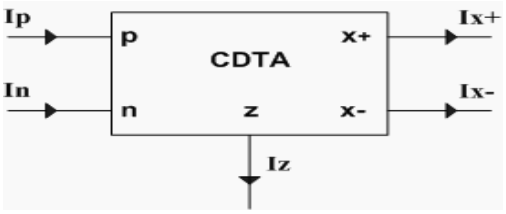

Figure 1 – The CDTA Element

$$V_p = V_n = 0 \qquad I_z = I_p - I_n$$
$$I_{x+} = gV_z \qquad I_{x-} = -gV_z \tag{1}$$

CMOS realization of the CDTA element is shown in Fig.2 [9]. This circuit can be operated down to supply rails of 0.75V. Another tempting feature is its very low input resistances at the p and n terminals which are close to 25Ω at moderate frequencies. This is satisfied using flipped voltage followers as current mirrors of the input stage. Further information about this cell can be found in [8]. Input resistance of the CDTA element, output resistance of FVF can be calculated approximately using the following equations [8], which give it as in the order of a few tens of ohms. SPICE simulation results give this value as 24.5Ω at 1MHz. After this frequency, it starts to increase as expected but it is still in acceptable limits till 100MHz.

$$R_{in_p} \approx \frac{1}{g_{m2}g_{m3}r_{o3}} \tag{2}$$

$$R_{in_n} \approx \frac{1}{g_{m8}g_{m9}r_{o8}} \tag{3}$$

On the other hand, one of the drawbacks of the circuit is the accuracy of the output currents because of this downside feature of output transconductance stage. More accurate transconductor stages can be used but this trades off supply voltage range or circuit compactness, which is an important factor for wide bandwidth operation. Transistor aspects of the circuit are given in Table 1.

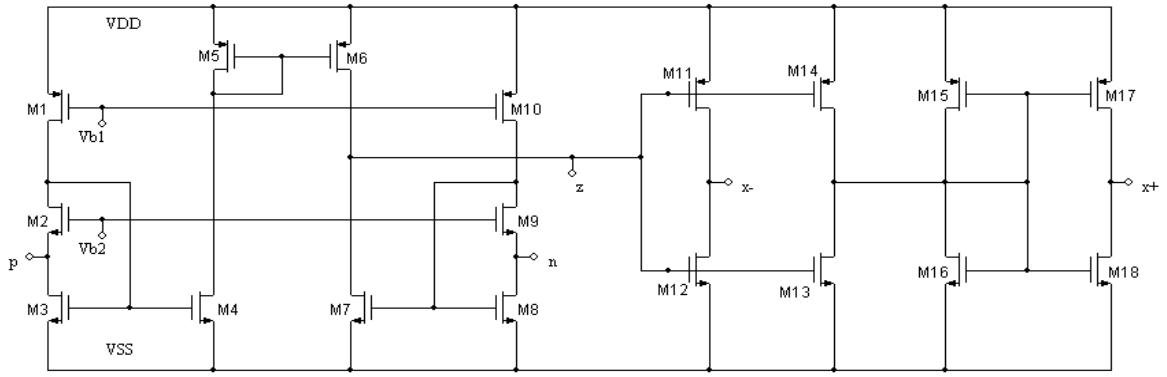

Figure 2 – CMOS Realization of the CDTA element

Table 1. Transistor Aspects

M1= 30µ / 0.7µ	M10= 30µ / 0.7µ
M2= 30µ / 0.7µ	M11= 50µ / 0.7µ
M3= 90µ / 2.1µ	M12= 4µ / 1.4µ
M4= 90µ / 2.1µ	M13= 4µ / 1.4µ
M5= 150µ / 3.5µ	M14= 50µ / 0.7µ
M6= 150µ / 3.5µ	M15= 50µ / 0.7µ
M7= 90µ / 2.1µ	M16= 4µ / 1.4µ
M8= 90µ / 2.1µ	M17= 50µ / 0.7µ
M9= 30µ / 0.7µ	M18= 4µ / 1.2µ

Further information about this low-voltage CMOS realization of CDTA can be obtained from [9]. Nevertheless, SPICE simulation results of this circuit are summarized in Table 2.

Table 2. Simulation Results

Supply Voltages	±0.75V
Bias Current	54µA
Technology	0.35µ AMIS
I_z/I_p (-3dB) Bandwidth	87MHz
I_z/I_n (-3dB) Bandwidth	20MHz
p input resistance	25Ω@1MHz
n input resistance	25Ω@1MHz
Power Consumption	0.37mW
Transconductance (g)	210µA/V
Biasing Voltages	Vb1=-0.2V, Vb2=0.3V
Input Offset Current	0.4µA

As seen from simulation results, 67MHz bandwidth difference between n and p terminal currents is caused by the current mirror high frequency poles. Input signal follows the path through these current mirror transistors from p to z. Biasing current of the circuit is chosen as a logical value that is enough to obtain acceptable circuit performance, at the same time, low power consumption.

3. QUADRATURE OSCILLATOR

Allpass filters are important circuit structures for analog signal processing applications. One of the application areas of allpass filters is quadrature oscillators. A quadrature oscillator can easily be obtained using one noninverting and one inverting allpass filter. CDTA-based, recently proposed allpass filter section are shown in Fig.3.

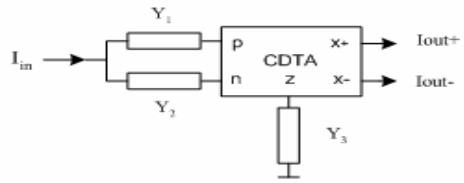

Figure 3 – CDTA-based allpass section

In the topology, while Y_3 determines DC gain of the filter, Y_1 and Y_2 determine whether the filter is inverting or noninverting. Choosing Y_1 as resistor Y_2 as capacitor, inverting allpass filter response is obtained at the negative output of the CDTA element. If Y_1=C, Y_2=G is chosen, noninverting allpass filter transfer function is satisfied at the negative output. g/Y_3 comes in front of this transfer funtion (4) as DC gain and can be set easily by choosing appropriate values for the impedances and transconductances of CDTAs.

$$\frac{I_{out-}}{I_{in}} = \frac{1 - sCR}{1 + sCR} \tag{4}$$

SPICE simulation result of this allpass filter response is shown in Fig. 4, where it is seen that ideal and simulated responses agree well. Using these allpass sections in a feedback loop, results in a quadrature oscillator where two outputs are in 90º phase difference.

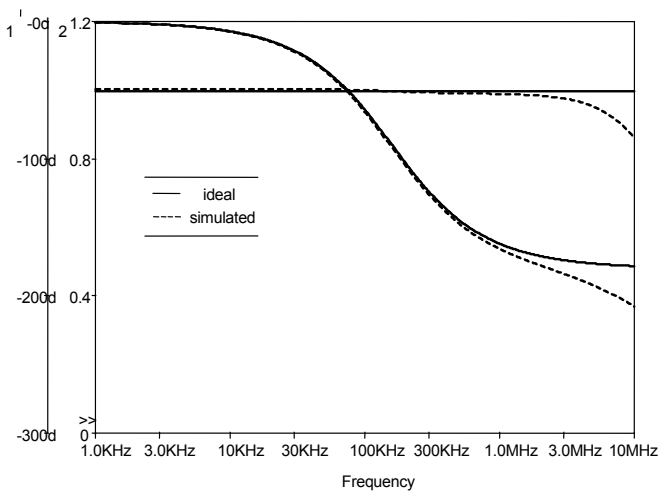

Figure 4 – Allpass section magnitude and phase responses

For the oscillator in Fig. 5, frequency of oscillation is given by

$$f_o = \frac{1}{2\pi\tau} \tag{5}$$

where τ is the time constant and equal to RC. In the circuit, R=R1=R2, C=C1=C2.

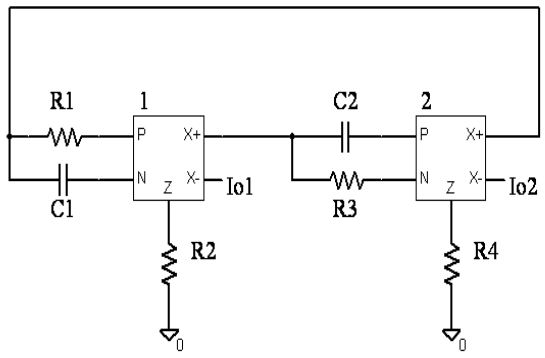

Figure 5 – CDTA-based quadrature oscillator topology

For the oscillator in the figure, passive element values are chosen as R1=R3=1kΩ, R2=R4=4.5kΩ, C1=C2=1nF. SPICE simulation result of the proposed quadrature oscillator is given in Fig.6. Using these values, frequency of oscillation is found as 159 kHz. SPICE simulation results give this value as 150 kHz, which is close to theoretical results. Small deviation from the theoretical results is probably caused by the parasitics at the input terminals of the CDTA element.

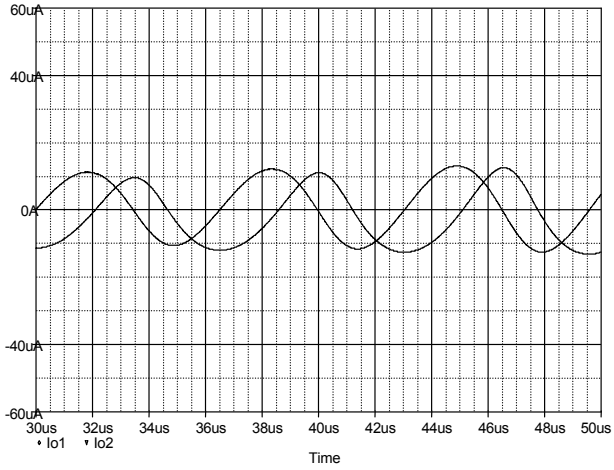

Figure 6 – CDTA-based quadrature oscillator responses

Oscillator circuit is loaded with an output resistor and its value is varied from 1Ω to 15kΩ. Variation of output voltage versus output resistance is shown in Fig. 7. As seen from the figure, it is possible to obtain output voltage signal close to supply voltage value.

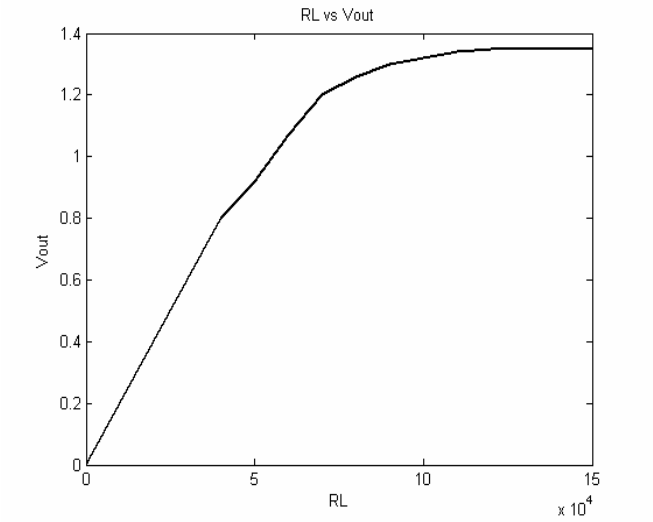

Figure 7 – Variation of output voltage versus load resistance

4. CONCLUSION

In this study, low-voltage CMOS realization of the CDTA element is given. Using this circuit in allpass filter sections, a quadrature oscillator is designed. Related SPICE simulation results are given. Proposed oscillator topology includes only six passive elements which is an improvement over its OTRA and Operational Amplifier counter parts.

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