Parallelisation of the Overlap-Add Block-Filter Algorithm for Image Processing

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Abstract

The utilization of multiple DSP systems for parallel processing in computationally demanding applications is growing fast. The field of 2-D imaging and multidimensional signal processing is a good candidate for parallel processing due to the large amount of low level computations required.
In this paper we present a 2-D parallel algorithm for the overlap-add digital block filter and a multiprocessor architecture suitable for image processing applications. We also investigate parallel processing systems in terms of performance and efficiency. The implementation of the 2-D parallel algorithm is discussed and results are given to show the performance of the parallel system compared to a single processor system.

1. Introduction

The growing importance of parallel processing is reflected by the large number of applications that embrace it [1,2,3], such as medical imaging, RADAR, SONAR, and image communications. The large processing power offered by parallel processing is thought to open the door for a whole new field of applications where intensive processing power is required for solving computationally demanding problems, and as physical limitations restricts the single processor system performance.

The block digital filtering approach is suggested to reduce the computational complexity of digital filtering systems, and increase parallelism. The 2-D parallel block filtering algorithm developed in Figure 1, converts the input block into a series of contiguous blocks of length (kxk) by means of a series-to-parallel converter algorithm, each input block is then processed simultaneously by a multiprocessor stage, the output blocks are then converted back into a single block by means of a parallel-to-serial converter algorithm.

2. 2-D Parallel Algorithm for Digital Block Filtering

The 2-D parallel algorithm developed for the block digital filtering approach is shown in Figure 1. The parallel algorithm is based on the overlap-add block filtering approach. In this algorithm the input block is decomposed into 4-sections of equal size according to the equation:

$$x(n_1,n_2)=x(k_1,k_2)+x\left(k_1+\frac{n_1}{2},k_2\right)+x\left(k_1,k_2+\frac{n_2}{2}\right)+x\left(k_1+\frac{n_1}{2},k_2+\frac{n_2}{2}\right) \quad (1)$$

where n_1 and n_2 are the input rows and columns, and $0\le k_1<\frac{n_1}{2}$, and $0\le k_2<\frac{n_2}{2}$.
Each term in the LHS of equation (1) represents a separate section of the input that will be processed independently on a separate processing element.
In the output stage the final output is reconstructed from the different outputs of the multiprocessor stage according to the equation:

$$y(l_1,l_2)=y(m_1,m_2)+y\left(m_1+\frac{n_1}{2},m_2\right)+y\left(m_1,m_2+\frac{n_2}{2}\right)+y\left(m_1+\frac{n_1}{2},m_2+\frac{n_2}{2}\right) \quad (2)$$

where $l_1=n_1+h_1-1$, and $l_2=n_2+h_2-1$, and h_1 and h_2 are the filter array rows and columns.
Each term in the LHS of equation (2) represents the output of a separate processing element; these outputs of size (m_1xm_2) overlap each other by the size of the filter array dimensions, which then gets added to the neighbouring blocks in the final stage.

3. Architecture for Parallel DSP's

The multiprocessor architecture used is shown in Figure 2. It consists of identical processing units (DSP-1 to DSP-4) operating simultaneously on separate sections of the input data. The control unit is the unit that receives the input image data and decomposes it into sub-blocks according to the 2-D serial-to-parallel algorithm given in equation (1), the sub-blocks then gets sent to the array of processors. The processing units work simultaneously on different sub-blocks, this helps reduce the problem of inter-processor communications, which tends to reduce the efficiency of multi-processor systems.

The multiprocessor architecture utilizes the SIMD (single instruction stream, multiple data stream) technique [4], to efficiently map the 2-D parallel algorithm onto the available processing elements for simultaneous operation. This helps reduce the problem of synchronization in the processor array. The processors in the processor array then fetch their data from the shared memory simultaneously, in which the different sub-blocks of the input image reside. The processed data from the processor array is then passed on to a final stage of processing where the reconstruction of the final output image from the sub-blocks is carried out. The reconstruction stage involves inter-merging the resulting sub-blocks using the 2-D parallel-to-serial algorithm in equation (2).

Besides the shared memory communication, which is mainly used for large data bulks, message passing between the different processors is also used in this system. This is done over the control bus to access the distributed internal memory of the processors. This gives the kind of flexibility required for inter-processor communications in multi-processing systems, and to satisfy the processing bulk and throughput required from such systems.

4. 2-D Fast Transform for Image Filtering

For the purpose of fast image filtering we used the row-column 2-D approach based on the 1-D split-radix Hartley transform (SR FHT) [5,6]. The fast Hartley transform was used because it has the cyclic convolution property and it is a real-to-real transform, which makes it memory efficient. It is also simpler to encode as the forward and inverse transforms are exactly the same.

The 2-D algorithm shown in Figure 1 is suitable for fast filtering applications – i.e. processing is carried out in the transform domain then transformed back to the time domain at the output stage.

5. Parallel Processing Performance and Results

The ASP-P15 DSP card is used for the implementation process. This card is the Quad-DSP version with 4-SHARC DSP processors on board. The DSP-card has a PCI interface and can be plugged in a host system, which then serves as an I/O device.

Tests are carried out on the system shown in Figure 2 in order to obtain practical results and be able to assess the performance of the 2-D parallel algorithm by calculating the speeding factor over the uniprocessor system. A 2-D image array of size (256x256) is used with a (256x256) 2-D filter array; FIR filtering was carried out by fast transforms using the 2-D fast Hartley Transform (2-D FHT), as follows:

- Image filtering using 2-D FHT on one DSP processor.
- Image filtering using 2-D FHT on parallel system using 4-DSP processor card, which is, configured as shown in Figure 2.

Table 1 below shows the results obtained for the two cases above:

Case	Cycles ($x10^6$)
Single DSP System	**41.25**
Parallel DSP System	**11**
Speeding factor	**3.75**

Table 1, Results for Single and Multi-Processor Systems.

As can be seen from Table 1, a high speeding factor is achieved, which is close to the number of processors used. This shows the validity of the 2-D parallel block-filtering algorithm and proves that the interaction between the algorithm structure and the hardware structure is near optimum.

6. Conclusion

In this paper we have presented and implemented a 2-D parallel algorithm for the conventional block digital filtering case based on the overlap-add method, and hardware architecture suitable for digital image processing. The system achieves a high speeding factor close to the number of processors used; some results are presented to reflect the performance of this system. The algorithm involves the decomposition of a large 2-D image filtering into smaller sub-block image filters, which are easy to manage and can be calculated in parallel to reduce computational complexity. The split-radix 2-D row-column fast Hartley transform (FHT) was used to implement the filtering stage. The FHT is a real-to-real transform that offers memory saving and simple coding.

7. References

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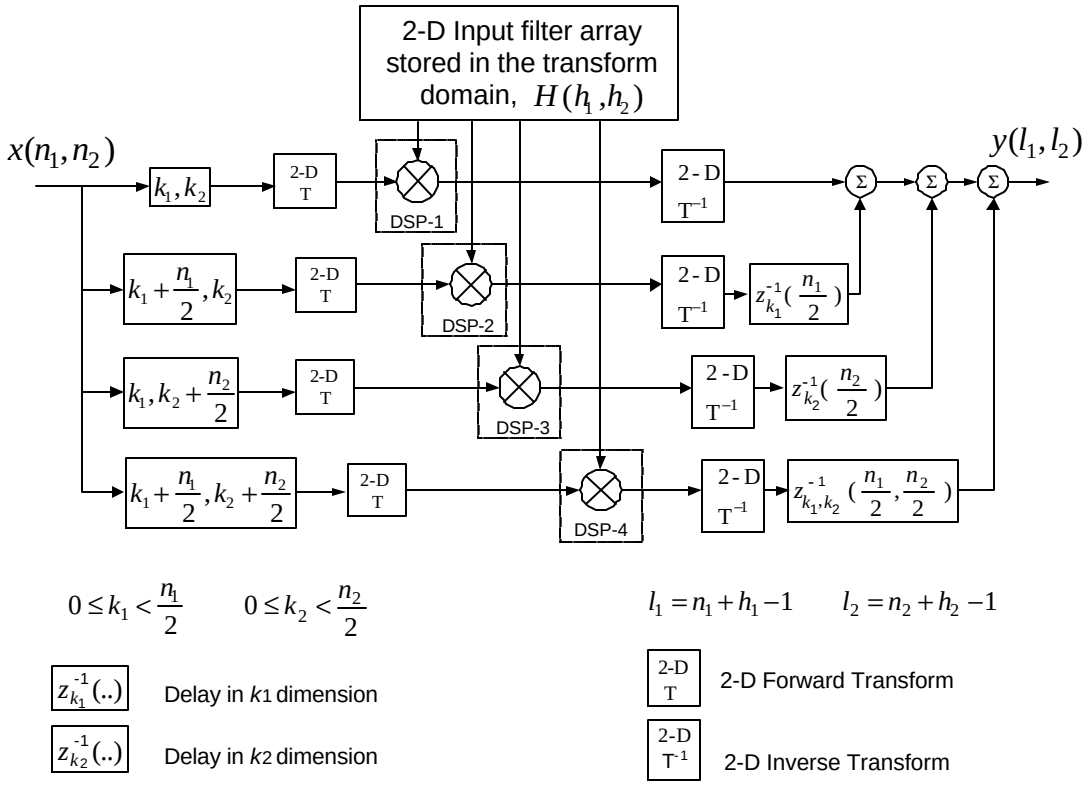

Figure 1. 2-D Parallel Block-Filtering Using Overlap-Add for Image Processing

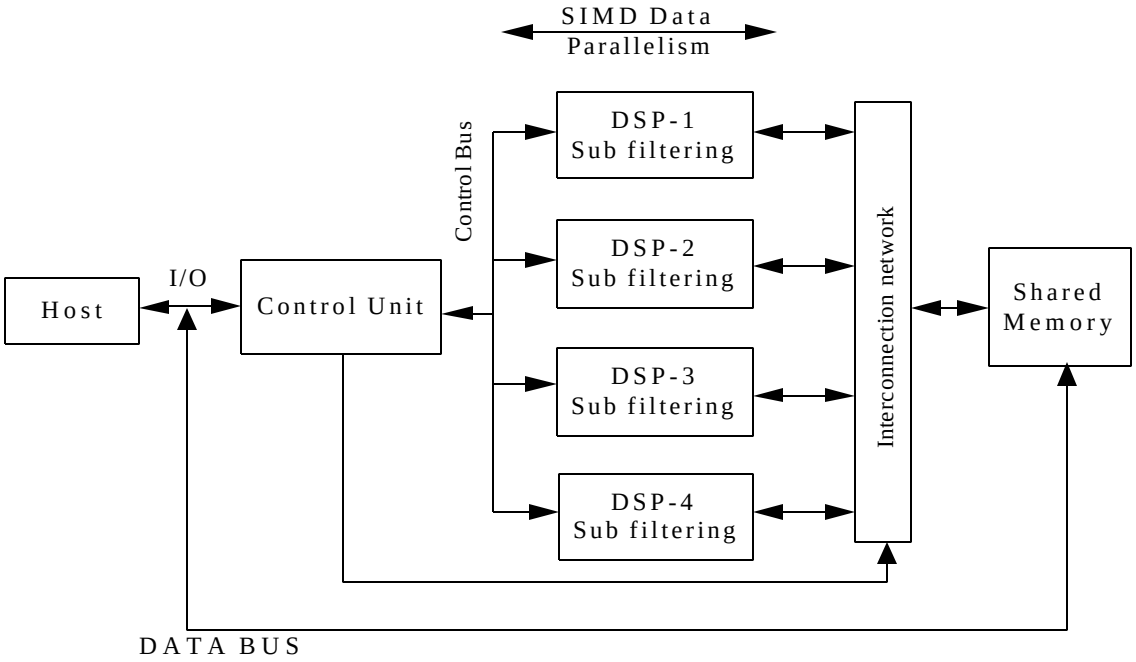

Figure 2. Multiple DSPs System Architecture for 2-D Parallel Image Filtering.