3G FDD Rapid Prototyping and Training

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ABSTRACT

In this paper the benefits of using a UMTS FDD physical layer compliant library for rapid prototyping and system modelling are presented. The paper also emphasises the use of this library for practical training. In order to illustrate these benefits three examples of common 3G structures and concepts are presented, implemented and studied: hybrid phase shift keying (HPSK) modulation; adjacent channel leakage ratio (ACLR) measurement; and a downlink reference measurement channel. A series of software simulation models associated with these examples are available for download from the world wide web.

1. INTRODUCTION

The FDD*Lib* is a UMTS FDD compliant library for the SystemView simulation tool which constitutes a useful platform for rapidly generating FDD simulation models, as well as for prototyping and testing of algorithms and architectures. This library has also been succesfully used for pragmatic 3G physical layer education.

This paper focuses on the the characteristics which make the library appropriate for the aforementioned tasks. These characteristics are: versatility; full spec compliance; friendly graphical user interface (GUI); and use of the same nomenclature and parameters as in the specs, thus providing a direct link between specifications and simulation models.

These characteristics are illustrated in three presented examples. Simulation models implementing these examples are available for download from [1]. These simulation models show how typical FDD structures can be rapidly built and, in particular, how to exploit the versatility of the FDD*Lib* in order to study the effect of parameters or elements of the system on its overall performance. Links are also given in [1] to download evaluation versions of the SystemView simulation package as well as the FDD*Lib*.

The paper is organised as follows: Section 2 introduces the modulation scheme used in the uplink spreading process: hybrid phase shift keying (HPSK) . The concept of adjacent channel leakage ratio (ACLR) measurement is presented in Section 3, where the effect of the root raised cosine (RRC) filter on this value is studied. Section 4 builds a downlink (DL) 64 kbit/sec (kbps) reference measurement channel [5] and studies its block error rate (BLER) performance, providing an insight in the performance of the turbo decoder for different values of signal to noise ratio. Finally, Section 5 presents the conclusions.

2. EXAMPLE I: HPSK MODULATION

This example shows the principles of HPSK modulation used in the spreading and scrambling process in the uplink (UL) as specified in [2], and the importance of correctly choosing the channelisation codes.

2.1 Aim of HPSK modulation

One of the main concerns when designing an uplink transmitter is to increase battery life, which can be achieved by increasing the amplifier efficiency. Amplifiers are more efficient when operating close to the saturation level, which involves reducing the peak to average power ratio of the signal before amplification.

HPSK is the spreading scheme used in the UL and attempts to increase battery life by reducing the peak to average ratio of the signal to transmit. Figure 1 shows a typical QPSK constellation with two types of undesired chip transitions which produce a high peak to average ratio: (1) 0 degrees transition which happens when two consecutive chips have the same value, observe the high amplitude peak in the constellation when this transition occurs; (2) 180 degrees transition which produces a zero crossing on the constellation and increases the peak to average power ratio.

The desired transition is the 90 degrees change between consecutive chips. For a typical QPSK system with random data in I and Q, the probability of a 0 degree as well as of a 180 degree transition is $1/4$. With HPSK, a 90 degree transition every second chip is forced, therefore reducing the probabilities of 0 and 180 degree transitions to $1/8$, and thus reducing the peak to average power ratio.

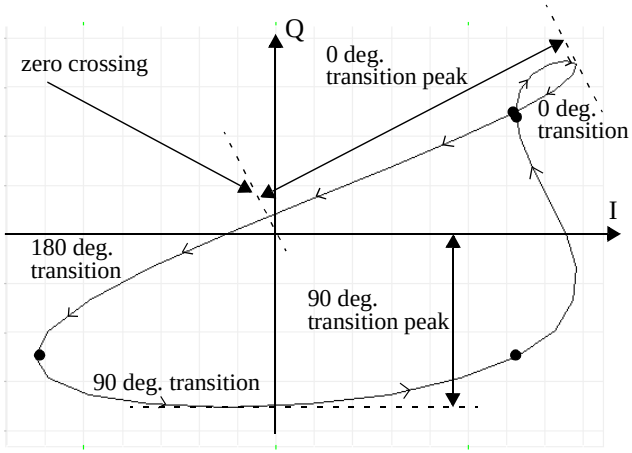

Figure 1: Examples of 0, 90 and 180 degrees transitions in a typical QPSK constellation

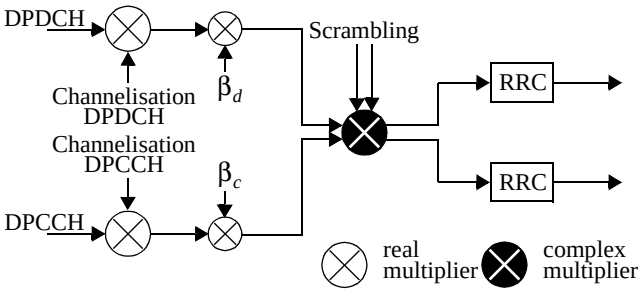

Figure 2: UL spreading for a single DPDCH and its associated DPCCH

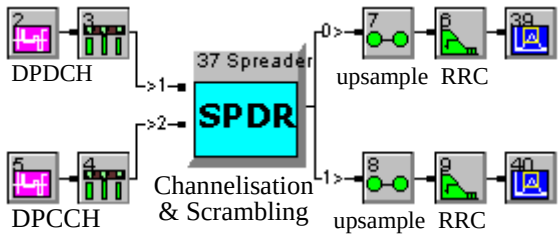

Figure 3: UL spreading for a single DPDCH and its associated DPCCH using FDD*Lib*

2.2 HPSK Modulation

The reduction of the peak to average power ratio provided by HPSK is achieved by using the appropriate channelisation and scrambling codes. Figure 2 shows the HPSK modulation scheme used in the UL with one dedicated physical data channel (DPDCH) and its associated dedicated physical control channel (DPCCH) as specified in [2]. The DPDCH and the DPCCH are channelised with different real codes and weighted with a value β_d and β_c respectively, the resulting signal is scrambled using a complex scrambling code. Figure 3 shows the implementation of this modulation scheme using the FDD*Lib*. This implementation includes RRC filtering (with an 8 times oversampled signal). Examples implementing this setup can be downloaded from [1].

The parameters of the spreader block are shown in Figure 4, this GUI allows the user to easily choose UL spreading and to enable or disable the channelisation and scrambling operations. These operations are fully parametrised and the channelisation codes number, the spreading factor (SF) for the I and Q channels, and β_d and β_c can be easily changed. The nomenclature used is the same as in [2].

The limitations imposed by the HPSK modulation in the codes are: the channelisation code for the DPDCH should be code number $SF/4$, while the DPCCH should always be channelised with code number 0 with SF = 256 [2] (this limits the rate of the DPCCH to a fixed value of 15 kbps); and a specific complex scrambling code has to be applied, information on how to generate this code is given in [2]. Using these codes we obtain the constellation of Figure 5 (a), while failing to use them we obtain the constellation of Figure 5 (b). Note how the number of zero crossings and the 0 degree transitions are increased.

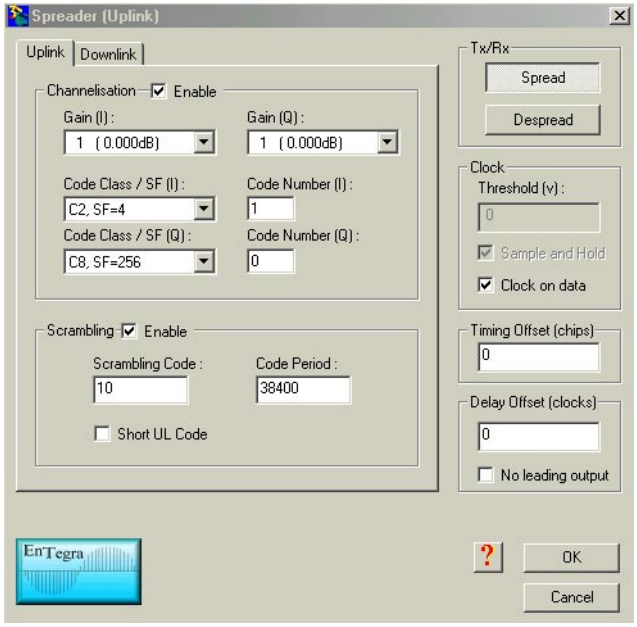

Figure 4: FDD*Lib* spreader token parameters

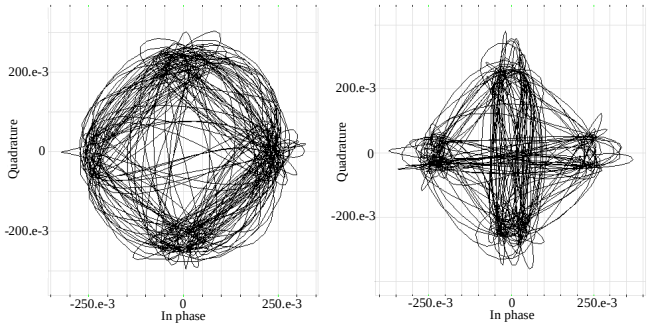

Figure 5: HPSK constellations; (a) using specified codes; (b) using wrong codes

3. EXAMPLE II: ACLR MEASUREMENT

In this example the design of an RRC filter which satisfies the required ACLR for a base station (BS) [3] is considered.

ACLR is defined as the ratio of the average power in the allocated frequency band to the average power in an adjacent frequency band. It measures how much power from a considered channel is being leaked into adjacent channels, and it is measured with an RRC filter with a roll-off factor $\alpha = 0.22$ [3].

The choice of the RRC filter is important, as it limits the bandwidth of the transmitted signal and attenuates unwanted components. The larger the number of RRC filter taps, the greater the attenuation outside the band of interest as shown in Figure 6, however more computations are required. Therefore, an RRC filter has to present a reduced number of taps and has to satisfy the ACLR requirements of Table 1.

In order to measure the BS ACLR, the system of Figure 7 is set up. The implementation using the FDD*Lib* is shown in Figure 8 (this system and information on how to build it can

BS adjacent channel offset below or above the considered carrier	ACLR limit
5 MHz	45 dB
10 MHz	50 dB

Table 1: BS ACLR limit values

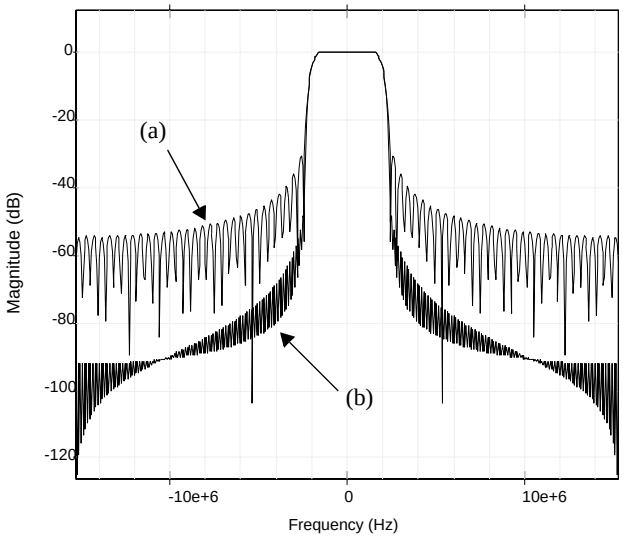

Figure 6: Magnitude response of two RRC filters with $\alpha = 0.22$: (a) 70 weights; (b) 256 weights

be downloaded from [1]). The BS is represented by a downlink (DL) generator token, which can generate DL FDD compliant dedicated physical channels (DPCHs) [4] and a number of common control channels [4] as well as multiuser waveforms. These channels can easily be enabled or disabled, and their power changed in the parameter dialogue box as shown in Figure 9. This token can also perform the RRC filtering, however, in our example the RRC filters are placed externally to the DL token for convenience.

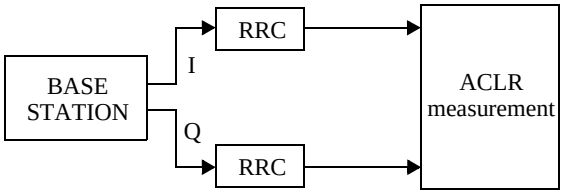

Figure 7: ACLR measurement set up

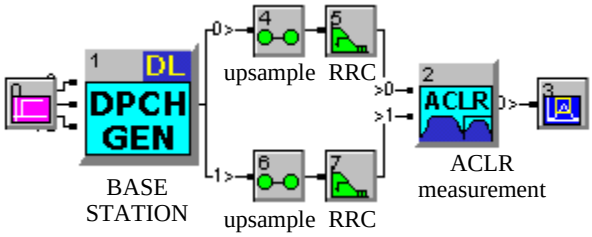

Figure 8: FDD*Lib* implementation of ACLR measurement set up

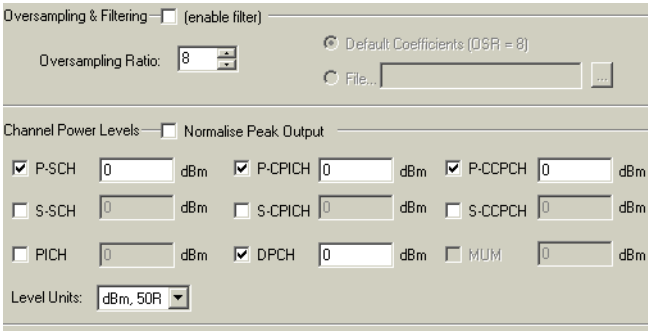

Figure 9: Detail of the DL generator token parameter dialogue box for common channels

Tests are carried out using RRC filters with 64, 70 and 128 weights. The ACLR measurement token provides the results shown in Table 2. Comparing these values with the required ones of Table 1 it can be concluded that a 70 tap RRC filter provides acceptable ACLR values.

No. of RRC filter weights	5 MHz	10MHz
64	43.65 dB	52.32 dB
70	45.97 dB	55.25 dB
128	55.69 dB	87.98 dB

Table 2: BS ACLR measured values

4. EXAMPLE III: DOWNLINK REFERENCE MEASUREMENT CHANNEL

This example implements a 64 kbps DL reference measurement channel [5]. This system transmits a dedicated transport channel (DTCH) at 64 kbps and its associated control channel (DCCH) at 2.5 kbps. The aim of this example is to build this reference measurement channel and the specific functions to implement are:

- transport channel generation;
- transport channel coding (cyclic code redundancy (CRC) coding; channel coding; rate matching; first interleaving; transport channel multiplexing; second interleaving;)
- slot segmentation and mapping of transport channel into dedicated physical channel (DPCH);
- channelisation and scrambling.

Parameter	DTCH	DCCH
Transport block size	1280 bits	100 bits
TTI	20 msec	40 msec
Error protection	Turbo coding	Conv. coding
Coding rate	1/3	1/3
Rate matching (block size)	input: 3888 bits output: 4014 bits	input: 360 bits output: 372 bits
CRC size	16 bits	12 bits

Table 3: Transport channel parameters

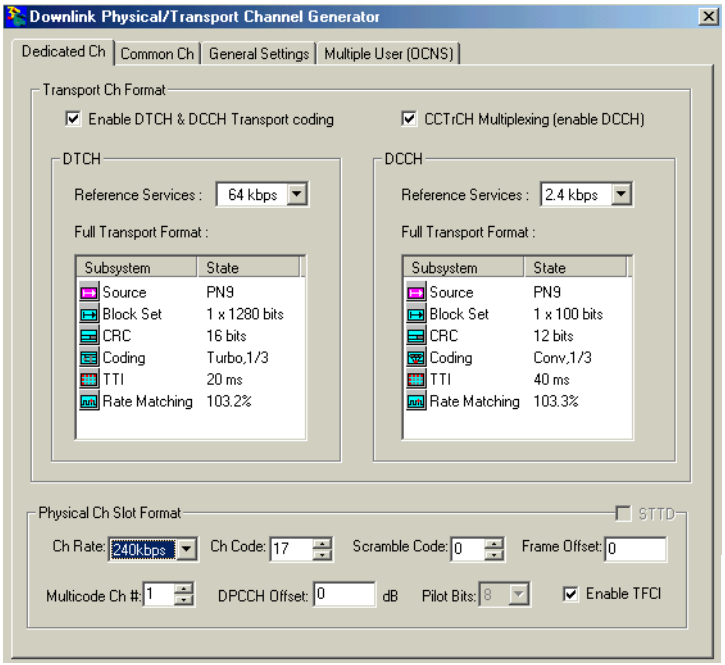

Figure 10: DL generator token parameter dialogue box

The resulting DPCH operates at a rate of 240 kbps [5] due to the overhead of channel coding. The transport channel parameters used are shown in Table 3, which are taken from [5]. These values can be directly mapped to the DL generator token parameter box as shown in Figure 10.

The full implementation of transmitter and receiver with an AWGN channel using FDD*Lib* is shown in Figure 11. The transmitter is implemented using the DL generation token (BS token), although all the different functions it performs can also be implemented using individual tokens, as shown in the examples which can be downloaded from [1].

The receiver implemented shown in Figure 11 includes the following elements: RRC matched filtering and a decimator to produce a chip rate signal; this signal is despread (dechannelised and descrambled) and with an integrate and dump structure the transmitted symbols are recovered; the resulting symbol sequence constitute the DPCH slots [4], whose fields (data and control) are demultiplexed; the obtained data is then passed through the second deinterleaver and the result is demultiplexed into DTCH and DCCH, which are finally transport channel decoded (first deinterleaving, rate recovering, channel decoding, CRC

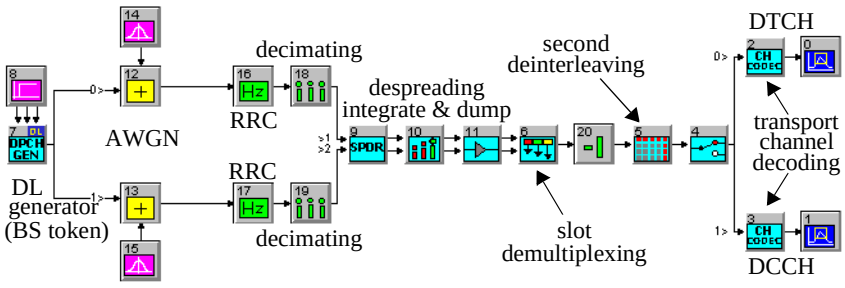

Figure 11: AWGN 64 kbps DL reference measurement channel implementation

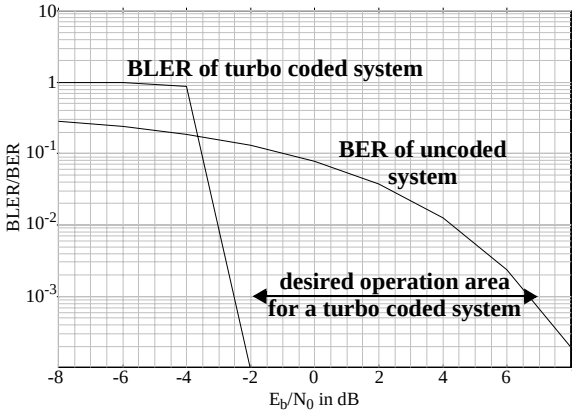

Figure 12: BLER of DL 64 kbps reference measurement channel with turbo coding and BER of uncoded system

decoding). All the tokens in Figure 11 are fully parameterised and the user can easily change the parameters associated and observe the effect they have on the performance of the system.

Results of BLER simulations are shown in Figure 12, where the values obtained using turbo coding are compared with the BER values from an uncoded system. Note the desired operation area when using turbo coding. For very low values of E_b/N_0 turbo coding produces high BLER values, which decrease to a very low value as E_b/N_0 increases.

5. CONCLUSIONS

The benefits of using the FDD*Lib* for rapid prototyping, system modelling and practical training have been presented. These benefits have been illustrated with three examples of common FDD structures and concepts: HPSK modulation; ACLR measurement; and 64 kbps DL reference measurement channel. A series of simulation models complementing these examples are available for download from [1] together with evaluation versions of the platform simulation software *SystemView* and the FDD*Lib*.

References

[1] http://www.**DSP***e*C.org/downloads/eusipco2002

[2] 3G TS 25.213. "Spreading and Modulation (FDD)", V3.6.0, Jun. 2001.

[3] 3G TS 25.104. "UTRA (BS) FDD; Radio Transmission and Reception", V3.7.0, Jun. 2001.

[4] 3G TS 25.211. "Physical Channels and Mapping of Transport Channels onto Physical Channels (FDD)", V3.7.0, Jun. 2001.

[5] 3G TS 25.101. "UE Radio Transmission and Reception (FDD)", V3.7.0, Jun. 2001.