EFFICIENT IIR SWITCHED-CAPACITOR DECIMATORS AND INTERPOLATORS

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ABSTRACT

The IIR switched-capacitor decimators and interpolators proposed in this paper are based on the polyphase decomposition of an M-th band IIR lowpass filter, and uses first- and second-order allpass switched-capacitor filters as basic building blocks, which operate at the lower sampling rate, reducing power consumption, capacitance spread and total capacitance area. The resulting switched-capacitor network has low sensitivity with respect to capacitance ratio errors, specially in the passband, where very low sensitivity is guaranteed by using structurally allpass filters. These properties have been verified by computer based sensitivity analysis, and an illustrative design example, considering realistic specifications for video communication applications, included in the paper, along with comparisons with other approaches reported in the literature. Laboratory results obtained with a prototype filter are shown as well.

1. INTRODUCTION

Considerable effort has been devoted to change the sampling rate of sampled-data networks by using interpolators and decimators, with the purpose of exploiting the changes in the signal bandwidth throughout the network [1]-[10]. Particularly important for switched-capacitor (SC) filters is the sampling ratio reduction, as it allows the use of operational amplifiers with smaller bandwidths, leading to low power consumption. Switched-capacitor decimators have been used in analog-digital interfacing circuits for effective sampling schemes of continuous-time signals [6]-[10], in such a way that time discretization of these signals is efficiently accomplished in two steps, as illustrated in Fig. 1. The output of the continuous-time anti-aliasing filter $H_a(s)$ is initially oversampled by some factor, say M, so that a low-Q anti-aliasing filter can be used. Therefore, in addition to providing interface with digital circuits, the SC decimator eases the requirements of the continuous-time anti-aliasing filter.

The design of SC decimators and interpolators has taken benefit from the wealth of knowledge developed for their digital counterpart [1]-[4]. An IIR SC decimator for a factor-of-M reduction of the sampling rate can be realized by making use of a polyphase decomposition of the lowpass IIR transfer function $H(z) = N(z)/D(z)$, as indicated in [2], [8]. The design procedure consists of multiplying numerator and denominator of $H(z)$ by an appropriate factor $Q(z)$, so that the modified transfer function can be expressed as

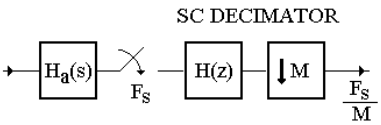

Figure 1: Efficient sampling scheme in two steps.

$$H(z) = \frac{N(z)Q(z)}{D(z)Q(z)} = \frac{N'(z)}{D'(z^M)} = \frac{\sum_{k=0}^{M-1} z^{-k} G_k(z^M)}{D'(z^M)}. \quad (1)$$

The main attractive feature of the resulting structure is that the SC decimator works now at the lower sampling rate F_s/M. The practical advantages of this approach, in terms of total capacitance area and capacitance spread, when compared to a conventional lowpass single-rate filter scheme [11] have been recently pointed out in an application for video communications [10].

In this paper a new IIR SC decimator is introduced. As in the scheme described above, it is based on the polyphase decomposition of a lowpass IIR transfer function, and the operational amplifiers work at the lowest sampling rate. The polyphase decomposition used here, however, leads to a highly efficient commutative structure for the polyphase filters [3], that is formed by first- and second-order allpass subfilters. This characteristic also yields good dynamic range and modularity. Although emphasis here is on SC decimators, the design of SC interpolators follows by duality [2]. In the following section a review of the basic concept is provided, and in Section 3 a SC implementation is presented.

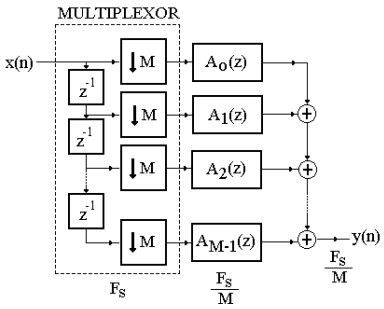

Figure 2: Efficient implementation of a decimator.

2. POLYPHASE DECOMPOSITION OF LOWPASS M-TH BAND FILTERS

A special case of the polyphase decomposition of a lowpass decimator for a factor-of-M sampling rate reduction can be written as

$$H(z) = \alpha + \sum_{k=0}^{M-1} z^{-k} G_k(z^M), \qquad (2)$$

where α is a constant which is usually chosen as $1/M$. A lowpass filter with a transfer function of the form of (2) is usually called an M-th band or Nyquist filter [4]. Under certain conditions, an M-th band IIR transfer function $H(z)$ can be decomposed as a sum of allpass transfer functions in the form

$$H(z) = \frac{1}{M} \sum_{k=0}^{M-1} z^{-k} A_k(z^M), \qquad (3)$$

as shown in Fig. 2, where $A_k(z^M)$ are stable allpass transfer functions.

In the case of a 2-band ($M = 2$) it has been shown that all Butterworth and elliptic odd-order half-band transfer functions can be analytically decomposed in the form of (3). For an M-th band transfer function with $M > 2$, a computer-aided design approach using a Remez-type algorithm to develop the decomposition has been reported in [3]. If phase distortion can be tolerated, then the resulting structure has the lowest complexity for the implementation of a decimator among all decimator structures reported in the literature. A correction filter is used to prevent aliasing distortion due to the transition and don't care bands [3].

3. SWITCHED-CAPACITOR REALIZATION

The scheme shown in Fig. 2 can be readily realized in SC technology, using as basic building blocks a demultiplexer, an adder, and allpass filters. One of the key features of the proposed SC network is the fact that the addition operation can be realized with high accuracy, ensuring a good performance in the stopband. The reason for this is the fact that the adder circuit uses only unit capacitance ratios, which can be implemented in such a way that random errors have a standard deviation smaller than 0.1% [13]. This aspect is particularly attractive in applications where phase linearity is part of the desired requirements, since linear phase can be approximated on the passband by the structure of Fig. 2 with one of the allpass blocks replaced by a delay [3]. In FIR based realizations of decimators and interpolators, different tap weight values have to be implemented by the output adder, compromising the delicate addition operation which has to take place in order to produce very low amplitude signals in the stopband [14].

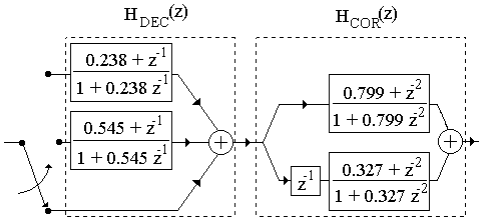

Figure 3: Block diagram for the video communication example.

Several SC allpass building blocks have been proposed in the literature [15]-[17]. In the decimator scheme presented here we use a cascade connection of first- and second-order allpass SC filters implemented in direct form [17]. While a high-order direct-form implementation of IIR SC filters should be avoided due to its high sensitivity characteristic [18], first- and second-order sections can be cascaded to exploit several useful advantages in MOS realizations, such as rejection of MOS amplifier noise and power supply noise below half the sampling rate, silicon area savings, and potential for time multiplexing [19]. In addition, the allpass direct-form filter used here has the important property that its transfer function remains allpass regardless any errors in the capacitance ratios that realize the filter coefficients. As a consequence, very low sensitivity is obtained in the passband, as shown next.

4. SIMULATION AND LABORATORY RESULTS

As an illustrative example, a factor-of-3 ($M = 3$) lowpass SC decimator has been designed, simulated on a computer and tested in laboratory using the ASIZ program [20]. The specifications, which are suitable for video communication applications, are as follows [11]: passband and stopband edge frequencies 3.6 MHz and 4.44 MHz, respectively, passband ripple less than 0.4 dB and stopband attenuation larger than 25 dB. The block diagram of the resulting decimator is shown in Fig. 3 for a decimation factor $M = 3$ and input sampling frequency of 48.2 MHz. The filter $H_{DEC}(z)$ implements the block diagram of Fig. 2, and the correction filter

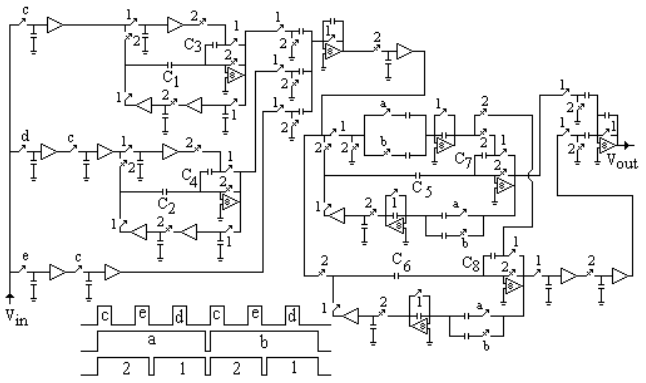

Figure 4: Decimator circuit and switching waveforms for the video communication example.

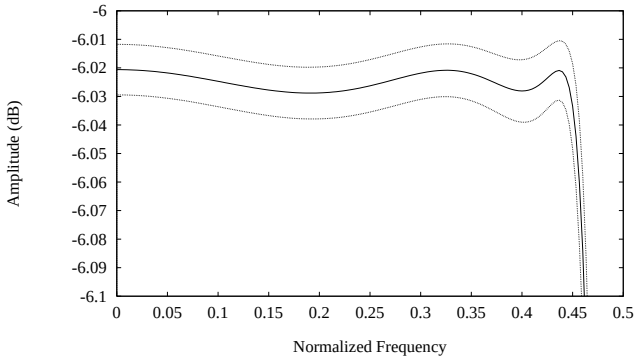

Figure 5: Sensitivity analysis of the proposed decimator.

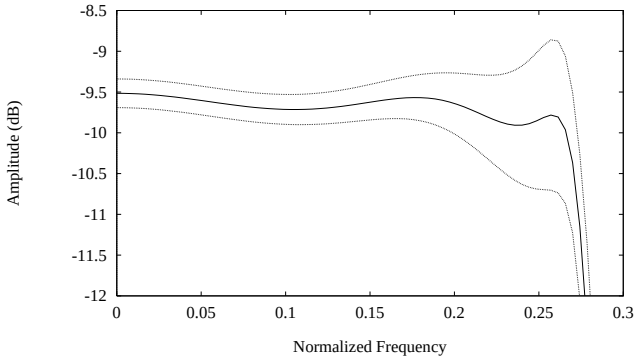

Figure 6: Sensitivity analysis of the decimator proposed in [11].

$H_{COR}(z)$ is a half-band filter used to reduce aliasing efects, as mentioned in the previous section. The corresponding SC network is shown in Fig. 4. The nominal passband ripple is 0.0081 dB and the nominal stopband attenuation is 28 dB.

A number of interesting features can be observed in Fig. 4. First, the (upper) forward path shown in Fig. 4 is shared by both the allpass filters that implement $H_{COR}(z)$. Second, for $H_{DEC}(z)$, $A_1(z)$ and $A_2(z)$ are first-order allpass transfer functions and $A_3(z) = 1$. Third, except for the capacitances $C_1 = 0.238$, $C_2 = 0.545$, $C_5 = 0.799$ and $C_7 = 0.327$, all the other capacitances are equal to 1. The capacitance spread is, therefore equal to 4.2. The total capacitance is 46.3 units. These figures compare favorably with a recent design [10] based on the polyphase decomposition given by (1), in which the capacitance spread is 8.19 and the total capacitance area is of 92.48 units. The number of active elements is larger in the proposed decimator: 9 op amps and 16 unit buffers, against 6 op amps used in [10]. It should also be noted, however, that unit buffers have much simpler structures than op amps, and have, in fact, been preferred in many SC filter implementations, as in [12], for instance.

Figures 5 and 6 show, respectively, results of sensitivity analyses obtained for the proposed decimator and the one reported in [10], considering errors with 1% standard deviation in non-unit capacitance ratios, and 0.1% standard deviation in unit capacitance ratios, as the latter can be realized with high accuracy, as noted in the last section. The upper and lower sensitivity curves encompass 68.3% of all decimators. It should be observed in Fig. 5 that the decimator proposed in this paper is still able to satisfy the original specification of 0.4 dB ripple in the passband, since the ripple indicated by these curves is never larger than 0.01 dB. In Fig.6, on the other hand, the ripple is 1 dB, as shown by the lower sensitivity curve. Even if 0.1% standard deviation error are used for all capacitances in the circuit proposed in [10], this ripple would be around 0.45 dB, which is still higher than the nominal ripple value. This large sensitivity is due to the fact that capacitance mismatches introduce different polynomial factors in the numerator and in the denominator of $H(z)$, and not the same $Q(z)$ as indicated by (1) in the ideal case.

A prototype decimator has been built using discrete components (LF351 op amps and CD4066 analog switches), and tested in the laboratory. Capacitance ratios have been adjusted to be within 1% of their nominal value. The input sampling rate used was 3 kHz. The measured amplitude frequency response is shown in Fig. 7, and has been obtained by using a HP3582A spectrum analyzer. The measured frequency response agrees very closely with the theoretical one.

5. CONCLUDING REMARKS

A new structure for the realization of IIR SC decimators and interpolators, using an allpass based polyphase decomposition of M-th band lowpass IIR transfer functions has been presented. Due to the use of structurally allpass filters as basic building blocks, very low sensitivity has been obtained in the passband. A design example for a factor-of-3 sampling rate reduction has been presented to illustrate the design process. Comparison with another structure recently resported in the liter-

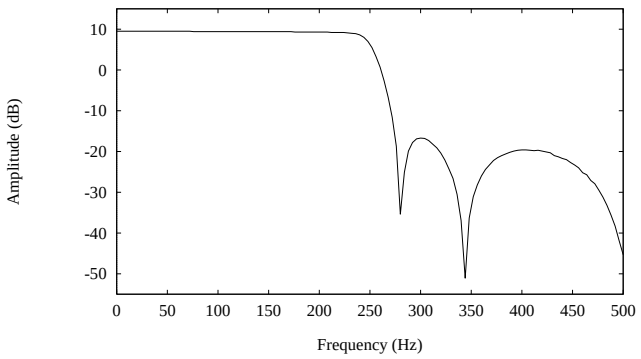

Figure 7: Measured frequency response of the proposed decimator.

ature has shown that the proposed decimator presents considerably lower sensitivity in the passband with respect to capacitance ratio errors, uses less capacitance area and has lower capacitance spread, at the cost of a larger number of active elements. Experimental results obtained in laboratory with a prototype decimator have also been shown.

ACKNOWLEDGMENTS

This work was supported in part by Conselho Nacional de Pesquisa e Desenvolvimento (CNPq, Brazil), and in part by a grant from the Rockwell International Corp.

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