A NEW STRUCTURE FOR VIDEO-RATE 2D SC FIR FILTERS

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ABSTRACT

Since Switched Capacitor (SC) circuits operate with discrete-time analog signals, it becomes rather attractive revisiting traditional video operations in the attempt of replacing systems currently implemented digitally with SC circuits, wherever possible. Indeed substituing the digital part for an analog one leads to substantial improvements with respect to power and area characteristics.
This kind of circuit variations poses a number of challeging problems mainly related to the fact that the circuit cloks are at video-rate. This work describes possible solutions to these problems exemplified by the SC realization, by standard monolithic CMOS technology of a 2-D low-pass filter designed for picture-in-picture (PIP) resizing.

1 INTRODUCTION

Switched Capacitor circuits, as discrete-time devices operating with analog (non-quantized) signals, can realize discrete-time systems as well as approximation of small-bandwidth continuos-time systems. Video systems, traditionally resorting to analog processing, offer a variety of situations where the discrete-time/analog nature of SC circuits can play useful services. Indeed they can realise, as integrated chips, analog pre- and post- filters, commonly implemented by discrete components [2]. Moreover SC circuits can eliminate A/D and D/A conversion blocks. SC solutions imply good area/power savings, with respect to traditional digital solutions.

The extension of SC technology to video applications requires overcoming a number of typical difficulties, the first of which being the bandwidth of the video-signals, which requires high sampling frequencies, not easy to achieve by current CMOS technology. This problem can be solved by the use of multirate structures [1]. A second difficulty is the tightness of the group-delay requirements, typical of video systems. Linear phase FIR filters offer a general solution to the group-delay problem. Finally some circuital non-idealities (such as finite resistance of switches in the ON state and real Op-Amps) must be carefully considered, expecially at high sampling rate.

A bidimensional FIR filter can be transformed into a monodimensional one [4], according to a specific technique described below. This allows to apply to 2-D filters the wide body of knowledge developed for monodimensional FIR filters.

The feasibility of the proposed video-rate SC bidimensional filters is demonstrated by an example of a 7x7 low-pass filter for PIP resizing.

This work has four sections: Section 2, after a brief introduction to multirate structures, explains the transformation of bidimensional filters into monodimensional filters and the implementation of the delay blocks by an analog RAM. Section 3 describes the implemented circuit; finally Section 4 presents the simulations results and the conclusions.

2 PROPOSED SAMPLED-DATA ANALOG STRUCTURE

As pointed out in the Introduction, the high sampling frequency required in video systems, represents a serious problem in the implementation of SC circuits, mainly because of the finite Op-Amp bandwidth. Multirate structures are a good cure to this problem, which allows for a substantial relaxation of the Op-Amps speed requirements. More specifically we adopt the Delayed N-Path structure [1] [2] [5].

Bidimensional FIR filters can be considered as a special case of monodimensional FIR filters, as firstly pointed out by Dudgeon and Mersereau for 2-D digital filters [4]. Indeed a MxN 2D filter can be interpreted as the juxtaposition of N monodimensional filters of M taps, essentially applying the scanning process to a bidimensional FIR filter structure. If the impulse response of the bidimensional filter is $h(m,n)$, defined on $\{0 \le m \le M-1, 0 \le n \le N-1\}$, we can define a reversibile transformation

$$g(l) = g(m + M \cdot n) = h(m,n) \qquad l = m + M \cdot n \tag{1}$$

Function $g(l)$ is an impulse response which can be interpreted as a monodimensional representation of $h(m,n)$ (Figure 1).

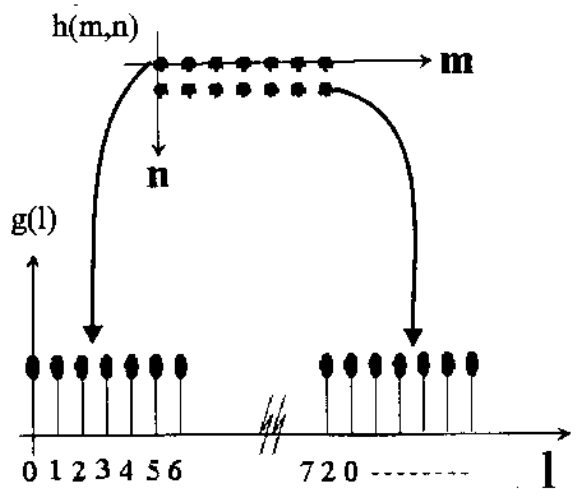


Figure 1: *1-D FIR filter g(l) equivalent to h(m,n)*

Unfortunately the straightforward application of this concept implies a very large number of delay lines in the signal path (of 720 samples each) which is very difficult to realise in the analog domain. Indeed various disturbances (such as offset voltages, clock feedthrough, etc.) may accumulate voltage errors. Unfortunately, with analog systems, signal recovery techniques are not applicable as with digital systems. Further delay elements are required by the FIR filter itself and by the multirate structure.

An alternate and easier way of realizing the needed delay elements is by means of an analog random access memory (ARAM) device, acting as frame memory. The bidimensional SC FIR filter architecture which results from the use of an ARAM is completely different from the FIFO based architecture used for monodimensional FIR filters (Figure 2), which corresponds also to the architecture of the 2-D filters obtained by the concept of Dudgeon and Mersereau. The use of the ARAM leads to structures reminescent of the architectures of general purpose DSP devices, characterised by two sections, one devoted to data storage (typically a RAM) and one to computation. Examples of the type of ARAM suited to the proposed 2-D SC FIR filter realization can be found in [3].

In conclusion the solution proposed for the implementation of 2D SC video-rate FIR filters adopts the multirate SC structure in order to relax Op-Amp speed requirements, it adopts a 2D-to-1D transformation for the FIR transfer function and it uses an analog RAM in order to implement the required long delay lines.

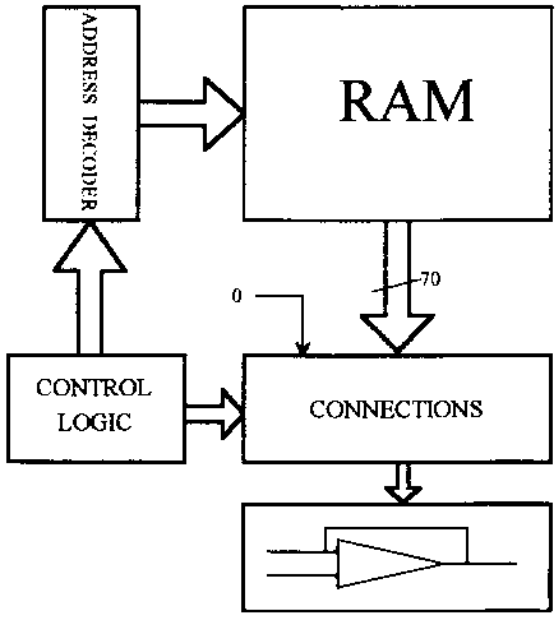


Figure 2: *2D SC FIR filter architecture based on the use of an ARAM*

3 A DESIGN EXAMPLE

In order to demonstrate the practical feasibility of the proposed solutions we implemented, in SC technology, a 7x7 FIR filter of the kind used within PIP devices. This is a low-pass filter suited to prefilter the video signal before reducing by three, both in the horizontal and in the vertical directions, the frame-size. PIP devices can fit up to nine different reduced frames in a standard video frame. The considered filter well represents the difficulties typical of video filters and in this respect the proposed solutions hold general validity.

Its sampling frequency is 13.5 MHz and its pass-band is 2.4 MHz, one third of the total available bandwidth. As a consequence of the use of the ARAM, the computational block of the SC FIR is an analog adder. The adder linearly combines the input samples according to weights corresponding to the FIR filter coefficients. The proposed structure is shown in Figure 3: the transfer function of the circuit can be expressed as

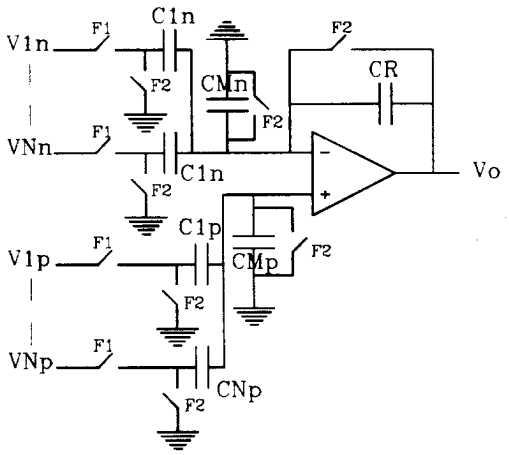
$$V_{out}(n) = \left[\frac{C_f + C_{M_n} + \sum_{i=1}^{N} C_{M_n}}{C_{M_p} + \sum_{i=1}^{N} C_{i_p}}\right] \cdot \quad (2)$$

$$\cdot\left[\frac{C_{1_p}}{C_f}V_{1_p}(n) + \ldots + \frac{C_{N_p}}{C_f}V_{N_p}(n)\right] - \sum_{i=1}^{N} \frac{V_{i_n}(n)C_{i_n}}{C_f}$$

Therefore if the ground capacitors satisfy to

$$C_f + C_{M_n} + \sum_{i=1}^{N} C_{i_n} = C_{M_p} + \sum_{i=1}^{N} C_{i_p} \qquad (3)$$

the circuit realises a linear combination, where the coefficient of the n-th input signal is the ratio between the feedback capacitor and the capacitor of the n-th input path. Therefore the filter taps are realised as ratio between two capacitors, as typical of SC circuits. Ratios between the largest capacitor and the smallest (a quantity usually referred to as capacitor spread), greater than 100 cannot be implemented with adeguate precision by current CMOS technology without excessive area requirements.



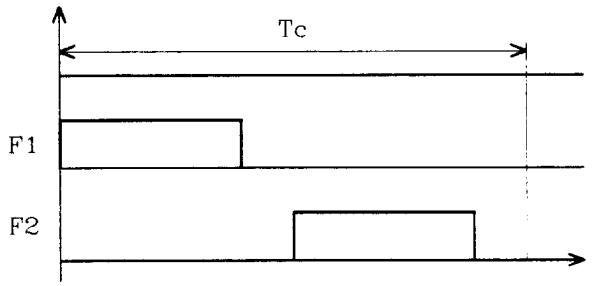


Figure 3: *Adopted multiplier/adder circuit*

Since the capacitor spread of the system is simply the ratio between the largest and the smallest filter coefficient, in our case a direct implementation implies a value of this parameter of approximately 6000, which is exceedingly high. Capacitor spread can be reduced by multiple stage implementation of the amplifier/adder circuit, where the first stage operates in parallel on the coefficients of comparable magnitudes, and the subsequent stages operate on the results of this sums with appropriate multiplying constants (K_i) in order to realize the correct transfer function. Figure 4 shows the structure obtained in this way. The various rectangular blocks indicate the switches and the capacitors configuration described above.

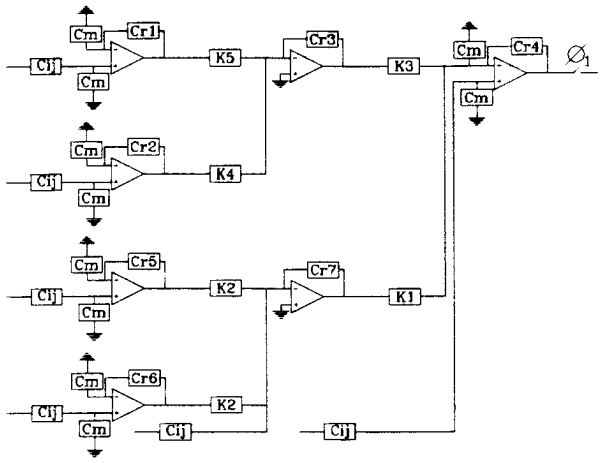


Figure 4: *Adopted multistage structure*

It is worth noting that this new structure is obtained from the iterative application of the following relationship to the filter transfer function:

$$H(z) = \sum_{n=0}^{L} h(n) \cdot z^{-n} = \qquad (4)$$

$$= K_1 \cdot \sum_{n \in N_1} \bar{h}(n) \cdot z^{-n} + K_2 \cdot \sum_{n \in N_2} \bar{h}(n) \cdot z^{-n}$$

where $\bar{h}(n) = \frac{h(n)}{K_i}$, $i = 1, 2$ and N1 and N2 represent a partition of [0, L-1] and where L is the number of filter coefficients.

4 RESULTS AND CONCLUSIONS

The proposed circuit was simulated assuming an ideal ARAM and considering various non idealities for the circuit components and various errors on their nominal values.

It was firstly considered that by current technology the ratio between capacitors, and so the coefficients values, can be controlled only up to 0.2%. This error can be modelled by assuming that filter coefficients are random variables whose average is their nominal value and whose standard deviation is equal to their nominal value times 0.002/3. More precisely, filter coefficients $h(n)$ were modelled as independent gaussian random variables with mean and variance

$$m_{h(n)} = E[h(n)] = \bar{h}(n) \qquad (5)$$

$$\sigma^2_{h(n)} = E[h^2(n)] - m^2_{h(n)} = \left[\frac{0.002}{3}\bar{h}(n)\right]^2$$

The transfer function was then calculated for 500 instances of the random variables and in order to have an

immediate display of the performance spread, the obtained results were superimposed on plots of the type shown in Figure 5. These plots show that the effects of the considered errors are within the prescribed tolerance.

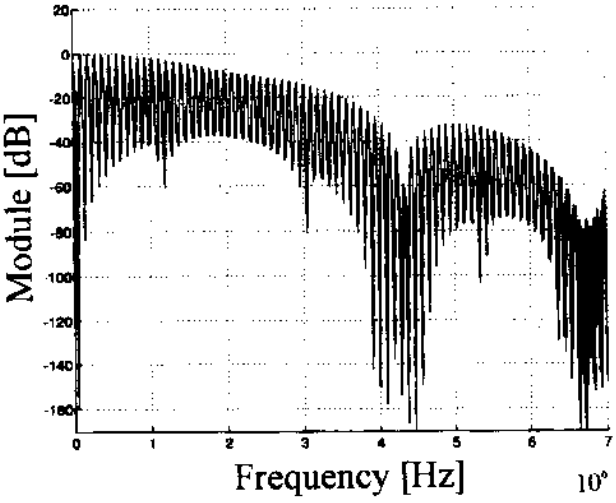


Figure 5: *Evaluation of the effects of the capacitor ratios error*

After validating the SC structure in this way, various circuit simulations were made in order to chek the effects of the most relevant non idealities of the used devices. We tested for the effects of the finite gain and bandwidth of the Op-Amps, of the output resistance of the Op-Amps and of the resistance of the switches in the conductive state. For simplicity Figure 6 shows the simulation of the cumulative effects of the considered non idealities, relative only to one row of the filter, but the results relative to the whole filter remain within the same tolerance range. Therefore the transfer function performance remains acceptable also with respect to these impairements.

The obtained results are rather promising because they indicate the possibility of realising SC video circuits with performance comparable with that of digital filters, but with lower power/area characteristics. Various refinements of the techniques presented in this work, aimed to further reduce circuital noise, are under study.

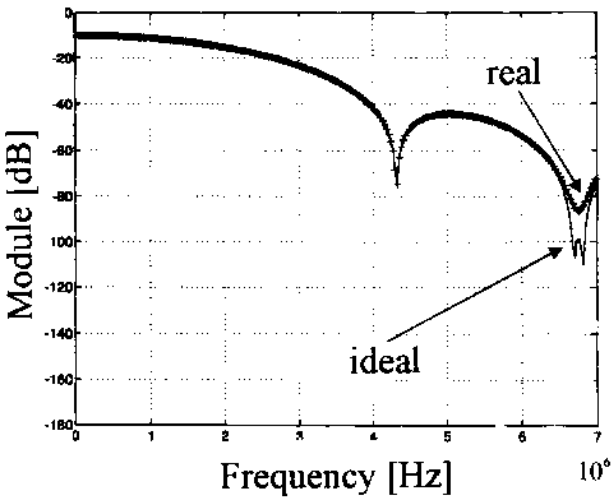


Figure 6: *Simulation accounting for non idealities of the used devices*

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