A Real Time ISO/MPEG2 Multichannel Encoder

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ABSTRACT

We describe the characteristics of a real time MPEG2 Multichannel Encoder based on a multi-DSP board. We discuss both the architectural base and the algorithm real time implementation. Due to the flexibility of the described card, realizations of other audio processing algorithms are also possible. A brief description of these implementations is also given.

1 Introduction

ISO-MPEG2 defines a generic audio-video standard coding with application to digital television (DTV), high definition digital television (HDTV), digital storage, and telecommunications. The audio part of this standard is mainly focused on the multichannel coding including the low frequency enhancement channel (the so called $5+1$ configuration).

In particular it relies a full backward compatibility with MPEG1 which provides the capability of an MPEG1 audio decoder to decode any MPEG2 bit stream. For high quality applications (i.e. contribution quality), the MPEG2 encoder can also provide an extension bit-stream to overcome the maximum bit-rate limitations of MPEG1 standard (384 Kbit/s).

It is well known that ISO-MPEG [1], [2] defines only the decoder structure; the encoder algorithm, which determines the final quality, can be improved and optimized by the designer. In addition a new standard (non backward compatible, NBC) for high quality professional applications is under definition in the MPEG working group.

In this context it is useful a very flexible hardware platform to follow the evolution of the standardization process and to progressively enhance the quality of the encoder implementation.

In this paper we present a VME card developed by Alcatel CRC to support audio compression and transmission in our professional audio and video equipment. In particular we describe the real time implementation of the MPEG2 Layer II multichannel coding algorithm.

It is also worth to mention that this realization has been successfully demonstrated in the frame of dTTb RACE project.

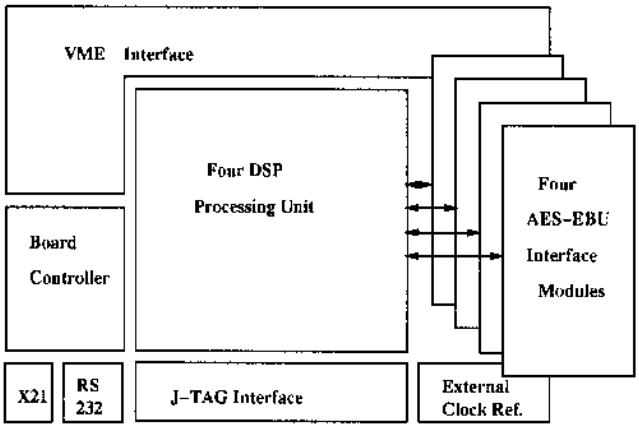

Figure 1: Hardware platform block diagram.

2 Hardware Platform

The objective of the development was to provide a very flexible HW platform capable support the current audio compression standard algorithms and their future evolutions. The adoption of a VME interface allows an easy integration of this board in a standard workstation environment making the applications development quite easy and efficient.

As illustrated in fig. 1 it is possible to identify the following main building blocks.

- Core Processing Unit
- Board Controller
- Audio Interface (AES/EBU)
- VME Interface
- Additional Interfaces (RS232,X21,J-TAG)

2.1 Core Processing Unit

The core processing unit is based on a multi-dsp architecture. We are currently using the 66 MHz version of

the Motorola DSP56002 digital signal processor [3], [4]. The four DSPs guarantee 133 Mips performance.

The external data busses are 24 bits wide, while the address busses uses $16 + 1$ bits. So for each processor 128K 24 bit words of fast (no wait states) static RAM are available.

The communication between the four processors is allowed by a four-ports static RAM (8K 24 bit words) that can be concurrently accessed. An additional communication channel is provided by the serial lines between processors (all DSP serial ports are connected to a powerful FPGA, the ALTERA EPF81188).

2.2 Board Controller

A fifth DSP56002 acts as the board controller. It loads from the flash memory the processors code and the FPGA's firmware, and after the bootstrap has been completed, it performs watch dog operations.

2.3 Audio Interface

The audio signals are received or transmitted through four balanced AES/EBU audio interface modules based on CS8411 and CS8401A Crystal devices. In addition four sampling frequency converters (Analog Devices AD1890) can be inserted between the AES/EBU interfaces and the processors in order to solve sample rate interfacing and compatibility problems with other digital audio equipment.

A Phase Locked Loop provides the ability to synchronize the board to an incoming signal or to an external clock source.

2.4 VME Interface

The VME interface is linked to the board controller through an 8K byte dual-port memory. So writing and reading this memory it is possible to control the board or to transit high speed signals between the board and the host workstation.

2.5 Additional Interface

The following reconfigurable input/output facilities are also provided.

- an RS 232 link
- the physical layer of X.21 (DCE-DTE)
- J-TAG interface on the five DSPs

In conclusion, this card has been designed with the goal to be highly flexible and reconfigurable; the DSPs can work both in parallel or in pipe-line (four-port memory allows a huge bandwidth of data exchange), and all the serial lines transit through Programmable Logic Devices. So it should be possible to implement here a wide range of audio compression algorithms.

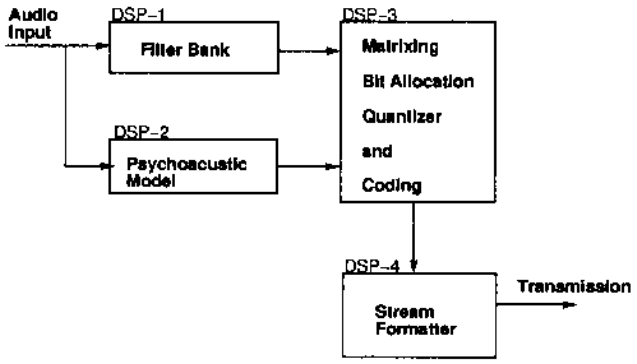

Figure 2: Generic MPEG encoding structure.

3 Algorithm Implementations

In this paper we illustrate the most significative implementations which has been realized up to now unsing the described hardware platform.

3.1 MPEG2-layer II encoder

We consider a multichannel ($5 + 1$) encoder compliant with the ISO 13818-3 standard [2]. Among a wide range of possible codec configurations, our goal was to realize a very high quality compression system for contribution applications.
At the present time the following features have been implemented.

- Matrixing
- Extension Stream
- Dynamic Switching
- Prediction (1,2 taps, 0...7 delays)
- Low Frequency Enhancement (LFE) channel

Considering the high computational power required, a key issue of the development was the algorithm partitioning among the four DSPs.

MPEG2-layer II encoder [2] works by pipelining the four DSPs (fig. 2). This is possible because the four-ports static RAM guarantees a fast, efficient and simple communication channel, So only a little fraction of time is wasted for the data transfers.

The main activities are split as follows (see time diagram in fig. 3).

- *DSP #1* sub-band analysis of the audio samples and down-sampling filtering for LFE channel (output:

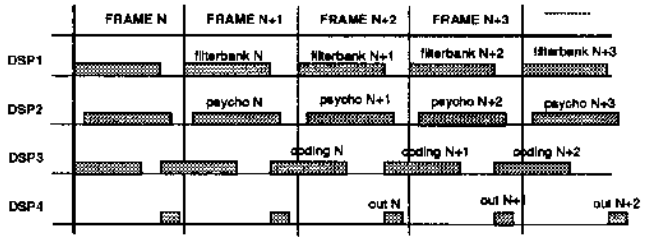

Figure 3: MPGE2 encoder timing.

filtered samples)

• *DSP* #2 psycho acoustic analysis of the audio samples (output: $5 + 2$ mask-to noise ratios)

• *DSP* #3 attenuation of the five sub-band filtered input channel MPEG-1 (stereo channels Lo,Ro) matrixing, full scale values computation, bit allocation, quantization MPEG-2 (multi channels) dynamic transmission channel allocation, inter channel prediction, full scale values computation, bit allocation, quantization.

• *DSP* #4 bit stream formatting

In order to emphasize the board flexibility, we briefly report on other algorithm implementations.

3.2 MPEG1-layer II encoder

Four MPEG1-layer II encoders work in parallel, that is each DSP receives a stereo program and produces a MPEG1 bit stream. So up to four independent MPEG1 bit streams are available.

3.3 MPEG1-layer II decoder

Four MPEG1-layer II decoders work in parallel, that is each DSP receives MPEG1 bit stream and produces a PCM stereo program. In this applications the board is clearly over dimensioned. The DSPs work at 30 % of the maximum speed.

3.4 MPEG2-layer II decoder

Only two DSPs are involved. The first one receives the MPEG transport packets, operates the demultiplexing and the time synchronization, and gives the audio bitstream to the second DSP which produces the $5 + 1$ audio PCM signals.

4 Conclusion

A real time implementation of a class of algorithms compliant with the ISO/MPEG-Audio standard has been presented.
The achieved results demonstrate that the described hardware architecture is particularly well suited for this kind of applications.

References

[1] K. Brandeburg, G. Stoll, Y. F. Dehery, D. J. Johnston, L. v. d. Kerkov, E. F. Shroeder. "The ISO/MPEG-Audio Codec: A Generic Standard for Coding of High Quality Digital Audio," *92nd AES Convention, Vienna 1992*, preprint 3336.

[2] ISO/IEC JTC1/SC2/WG11 MPEG, Committee Draft ISO 13818-3

[3] MOTOROLA DSP56000 Digital Signal Processor Family Manual

[4] MOTOROLA DSP56002 Digital Signal Processor User's Manual