THE IMPLEMENTATION OF A HIGH-SPEED DATA ACQUISITION SYSTEM FOR A DSP-BASED INSTRUMENT OPERATING IN REAL-TIME

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ABSTRACT

This paper deals with the hardware and software design and implementation of a modular DSP based instrument, which allows real-time measurements to be carried out. It is based on a TMS320C40 DSP, and on a modular high-speed data acquisition system, described in detail. Experimental results showing the system performance are also included in the paper.

1 INTRODUCTION

The Digital Signal Processor (DSP) technology exploits the superior features and benefits of digital electronics, such as reconfigurability, stability and noise immunity, in comparison with analog methods of processing real-world signals. These kind of devices are high performance processors which internal hardware is designed to execute quickly successive multiply-shift-add operations. They are then suitable to implement digital filters, FFT, speech or imaging processing and more complex data processing algorithms [1].

Sophisticated measurement and control applications benefit from the use of high performance DSPs [2, 3], where the time required for completing the tasks depends on the duration of: the input signal acquisition (A/D), the data processing (DSP), the output signal generation (D/A), in case the system must supply analogue responses.

Then, the primary key to obtain maximum performance in real-time applications of such systems is the design of an hardware that can acquire and process signal samples as these are received from the source, rather than storing them in buffers for batch-mode processing [4]. Efficient implementation of DSP hardware demands an appropriate architecture for the I/O hardware, in order to overcome this bottleneck.

This paper describes the architecture and a prototype implementation of a modular data acquisition system, for a DSP based measuring instrument. Some hardware and software issues associated with the design and the investigation of the dynamic behaviour of the system are presented, in order to highlight the achievable accuracy and speed of execution.

1. HARDWARE DESIGN

The proposed measurement system, sketched in Fig.1, is essentially composed of:

- high-performance data processing system, based on the TMS320C40 DSP;
- analog I/O channels, for the external analog signal acquisition and generation;
- interface circuits and communication protocol to interface the DSP to the I/O channels.

In the following these blocks are described in detail.

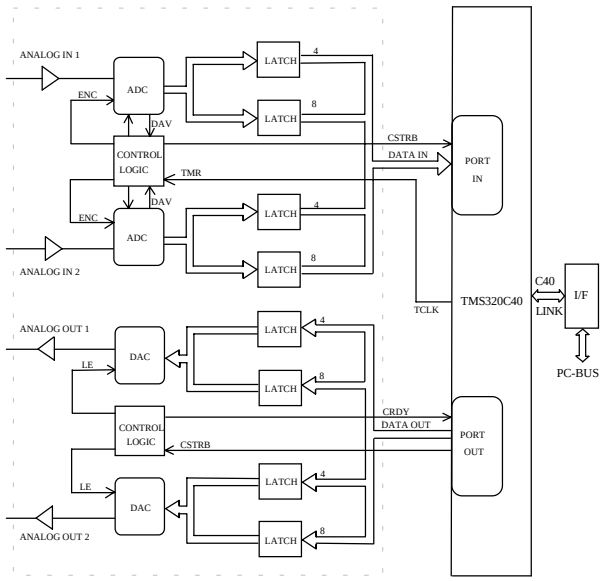

Fig.1 - Functional block diagram of a DAS module of the instrument.

1.1 Data Processing System: TMS320C40

The instrument adopts a Texas Instruments TMS320C40 DSP, and specifically the Transtech TTM60P-C40 TRAM board mounted on a IMS B008 carrier and hosted on a IBM-PC.

The TMS320C40 is a 32 bit floating point RISC DSP, 40 MHz clocked, capable to do up to 40 MFLOPS. It has a high concurrent architecture: 7 different internal buses (2 program buses, 3 data buses, 2 DMA buses) [5]. Two internal timers are also available, whose reference clock may be internal (the CPU clock) or external.

With its 6 high-speed parallel I/O ports (each of them with up to 20 Mbyte/s), it is designed to make it easier to interface either other processors (so realizing complex point to point architectures) or, like we did, A/D and D/A converters. Each port is software configurable as input or output and provides an high-speed link, with 8 parallel data bits (our data bus) and 4 lines to control the communication: CREQ (request),

CACK (acknowledge), CSTRB (strobe), CRDY (ready) [5].
Furthermore, the DSP communicates with the host personal computer via one port link, where an user interface is implemented.

1.2 The Analog I/O Channels

Data Acquisition System

In the proposed instrument, the Data Acquisition System (DAS) is composed of analog input and output modules.
Each Analog Input module includes two 12 bit A/D converters. Signal conditioning is realized with an active RC filter which cut-off frequency is strictly related to the sampling frequency. The adopted A/D converters (AD1671) operate with a sampling rate of up to 1.2 MHz (2 channels) or up to 2.4 MHz (1 channel). The chosen 12 bit A/D resolution is a compromise between the acquisition accuracy and the noise level of the input signals.
The Analog Output module includes two 12 bit D/A converters (AD9713), operating with an update time of 35 ns and linked to another DSP port.
To start the A/D and the D/A conversions and to free ourselves from the use of an external pulse generator, one of the two DSP internal timers (TCLK) is used: it produces output pulses whose repetition frequency mainly depends on the applied measuring algorithm and it is software programmable. Both input and output operations are controlled by the same sampling signal.

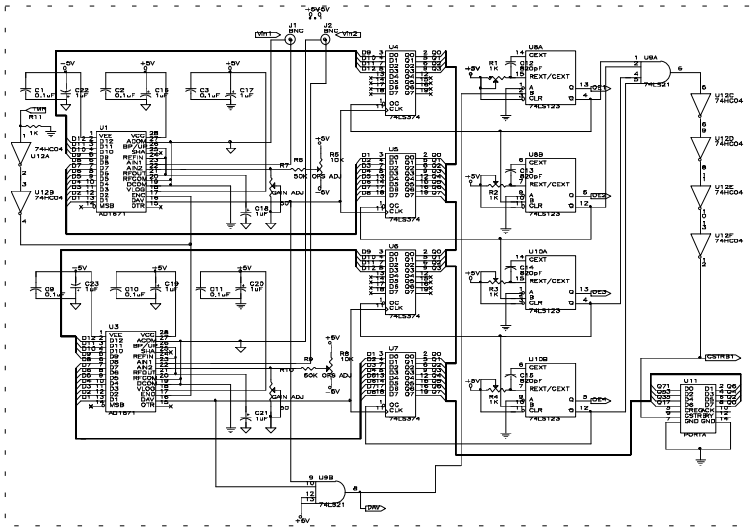

Fig.2 - DAS input module.

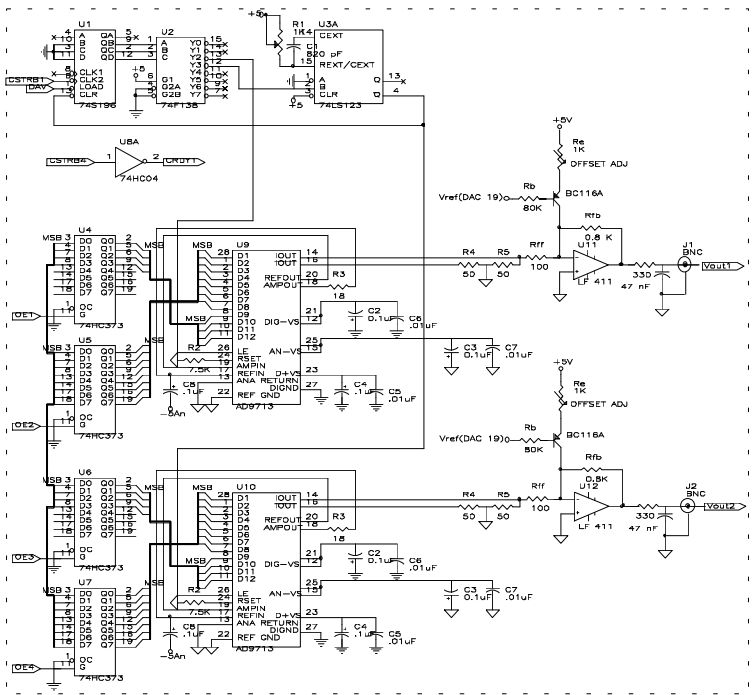

Fig.3 - DAS output module.

1.3 Interface circuits and communication protocol

Suitable circuits interface the data acquisition system to the DSP. They allows both the A/D and D/A converters to be linked to the DSP, handshaking the data exchange. The 12 bit data are transferred on the input and output data buses in the 8+4 bit way.
The proposed instrument executes concurrently the two analog input signal acquisitions and the two output signal generations. Input and output are software managed, by programming the port control registers.
The two 12 bit A/D output samples are latched in four 8 bit D-latches, which output buses are linked to a DSP port (see Fig.2). Four suitable signals control the latches input-output mode, to send data to the DSP input port bus at the right time. These signals are generated starting from the rising edge of the A/D end of conversion signal, the DAta Valid (DAV).
The acquisition of the 32 data bits in the input port is managed by a strobe signal (CSTRB), which is composed of 4 shifted pulses: corresponding to each negative edge, the DSP acquires 1 byte per time. This signal is generated starting from the latch control signals, delayed for 20 ns to compensate the latch delay time. According to the implemented hardware, the data byte sequence on the bus is: LB1-HB1-LB2-HB2. A complete read cycle allows both the A/D converters output to be read.
To interface the DSP output port to the D/A converters we need of the CRDY signal. Corresponding to rising edges of this signal, the DSP writes the 32 bit data, one byte per time. In order to simplify the hardware design, the CRDY was obtained by inverting the strobe signal CSTRB (see Fig.3).
The 32 bits DSP data should be demultiplexed to each D/A converter, as 4+8 bit. To avoid loading data on the DACs before the end of C40 write cycle, the output section latches are level sensitive and not edge sensitive.

The DACs output current (0÷22 mA) is converted in a balanced voltage with a circuit based on a transconduttance amplifier. A low-pass filter with the same bandwidth of the input anti-aliasing filter has also been included.

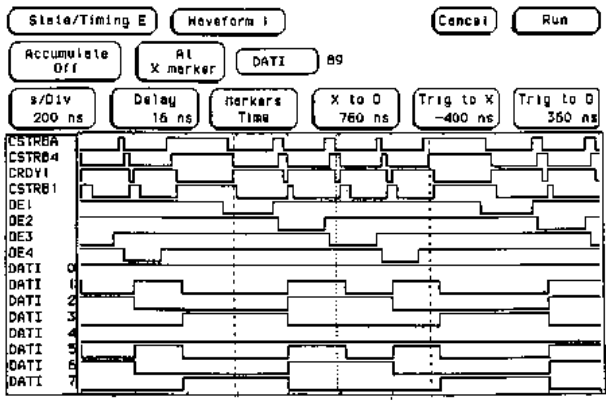

Fig.4 - Timing diagram for an I/O operation.

2 SOFTWARE DESCRIPTION

A special software library has been created in order to supply a kernel driving software. Once available, this kernel will simply have to be linked to the adopted real-time software, thus enabling a read cycle from an input port and a write cycle to an output port. The software drivers have been written in C language.

The input driver gets as a parameter the number of read cycles N and the requested sampling frequency; it will return the 2N analog input values from the two channels. When N=1 a single data is acquired. To do this, we need to:

- stop the timer;
- stop the input port and clear the input port queue;
- set-up the timer frequency and restart the timer;
- acquire the N data from the input port register;
- extract the 2N floating conversion results;
- store them in memory.

The output driver gets the processed floating values and send them to the required output channel. To do this, it will:

- read from memory the N floating output data and convert them in binary format;
- send data to the output port.

3 DYNAMIC BEHAVIOUR

In order to verify the dynamic behaviour of the implemented measuring instrument, we acquired a test wave produced by a high accuracy sinusoidal generator. A coherent and prime sampling was adopted to maximize the number of different codes at the A/D output, in order to analyze all the operating working conditions. The test sampling frequency f_c ranged from 250 kHz to 1 MHz. The obtained signal to noise ratios are reported in the waveforms of Figg.5,6.

As it appears, the increase on the sampling frequency f_c did not produce a significant growth on the noise level, which was always under the -60 dB level. The tests showed similar results on both the channels.

Beside, from the S/N ratio we deduced the effective number of bit *n*, by considering the following relation between S/N and *n*:

$$S/N\ (dB) = 6.02n + 1.76\ dB.$$

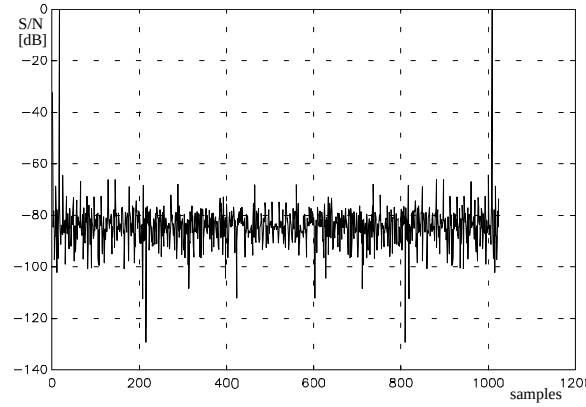

Fig.5 - Signal-to-noise ratio for f_C=250 kHz.

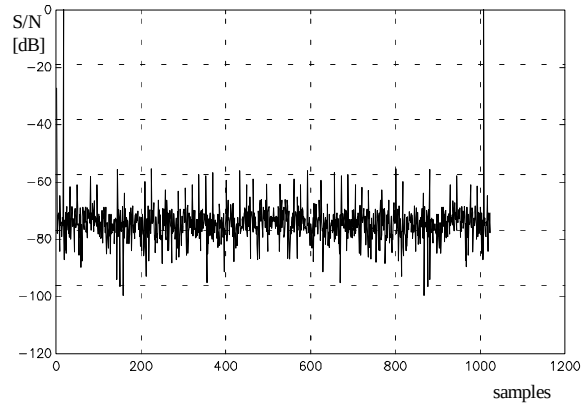

Fig.6 - Signal-to-noise ratio for f_C=1 MHz.

The effective bits obtained at different sampling frequencies, for both the channels, are reported in the following table:

Table 1 - Effective bits at different sampling frequencies.

	CH1		CH2	
f_C [kHz]	S/N [dB]	Effective bits *n*	S/N [dB]	Effective bits *n*
100	62.1	10.1	62.5	10.1
250	62.0	10.0	62.1	10.0
500	61.4	9.9	62.3	10.0
1000	57.2	9.2	58.5	9.5

As shown, for frequencies lower than 500 kHz *n* is about 10 bits. Anyway, when f_c significantly increases (around 1 MHz), *n* is about 9.2÷9.4 bits, showing the good performance of the data acquisition system, also for relatively high frequencies.

Further tests have been executed by applying a loopback technique. A discrete sinusoidal wave was numerically generated inside the DSP and it was sent to an output channel. Analog output voltage was applied to an input channel and acquired by the DSP, implementing in this way a closed-loop chain. The

acquired input data were compared with the generated ones: the obtained difference ε, is plotted in Fig.7.
As it appears, a low offset error is present, even if it may be compensated during the data processing. In Table 2 the closed loop error ε and the error after the compensation ε_{SW} are reported at different sampling frequencies f_c.

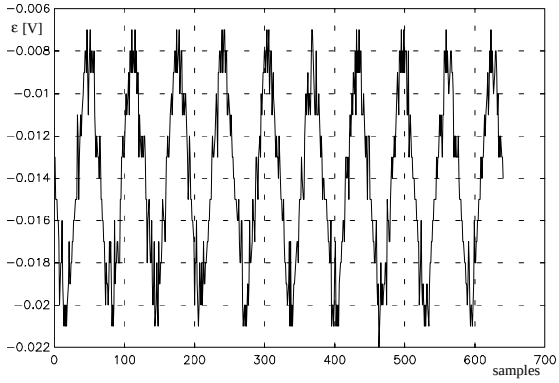

Fig.7 - Loopback error at f_C=64 kHz.

Table 2 - Closed loop error ε at different sampling frequencies.

f_C [kHz]	ε [%]	ε_{SW} [%]
64	0.40	0.13
100	0.82	0.44

As concerning the I/O timing, for the input operations, we have to consider two basic time intervals: (i) the A/D conversion time t_{ADC} (the time elapsed between the start of conversion pulse ENC and the end of conversion pulse DAV for both the ADCs) and (ii) the acquisition time t_{ACQ} (the time required by the DSP to complete a read cycle from the port). The t_{ACQ} is essentially the time interval needed to generate the four pulses signal CSTRB. Summarizing, the time required to complete the input operation is:
$t_{INP}=t_{ADC}+t_{ACQ}$.
In Fig.8 it results: t_{INP} = 1.620 μs, t_{ADC} = 860 ns, and t_{ACQ} = 760 ns (see markers).
To complete the output operation, the time t_{ST} is needed: this is the time elapsed from the negative edge of LE (the DAC start of conversion) to the completed settling of the DAC output. The measured t_{ST} time was 36 ns, for the current output, and 420 ns for the voltage output. This means that the available output frequency is greater than 2 MHz.

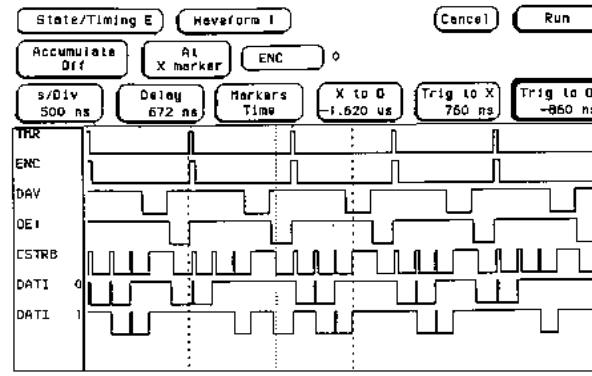

Fig.8 - Input timing diagram for an analog channel.

5 CONCLUSIONS

In the paper a modular Data Acquisition board for a DSP TMS320C40 is presented. The analog input and output channels make it fully general purpose for many real-time applications.
The dynamic behaviour for the two analog input channels and their input time are analyzed. The dynamic performance is evidenced with the effective number of bits, never lower than 9.2. The input time for the two channel input samples is 1.620 μs and the sampling frequencies available are up to 1.2 MHz, upgradable to 2.4 MHz if only one input channel is considered. A loopback test has given an error lower than 0.8%, thus evidencing the good accuracy reached by these analog channel interfaced to the DSP.

REFERENCES

[1] A.V.Oppenheim, R.W.Schafer, *Discrete-Time Signal Processing*, Prentice-Hall Inc., 1989.
[2] G.Bucci, C.Landi: "On-line Power Measurement in Non-Sinusoidal Condition By Using A FRLS Algorithm", in *Proc. of IMEKO-TC4 '95*, Prague (Czech Republic) Sept. 13-14 1995.
[3] A.E.Gaiarsa, D.W.Capson, "Real-Time Measurement of Corner Position in Binary Images", *IEEE Trans. On IAM*, V.43, N.4, 1994.
[4] G.Bucci, A.Germano, C.Landi, "Real-Time Transputer-Based Measurement Apparatus: Performance Testing", IEEE Trans. IM, Vol.43, N.2, Apr.1994.
[5] "TMS320C4X User's guide", Texas Instruments, May 1992.